REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Make change to the $V_{SL(0)}$ min limit from 1.24 V to 1.26 V as specified under Synchronization section of Table I. Update document paragraphs to current requirements. - ro	18-10-18	C. SAFFLE

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A	A	A	A	A			
	PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.dla.mil/landandmaritime**
Original date of drawing YY-MM-DD 13-04-15	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	TITLE MICROCIRCUIT, LINEAR, 4.5 V TO 60 V WIDE INPUT SYNCHRONOUS PWM BUCK CONTROLLER, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/13607**
	REV **A**	**PAGE** 1 **OF** 14

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

AMSC N/A

5962-V104-18

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 4.5 V to 60 V wide input synchronous pulse width modulator (PWM) buck controller microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/13607	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TPS40170 -EP	4.5 V to 60 V wide input synchronous PWM buck controller

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	JEDEC MO-241	Plastic quad flatpack no-lead

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Input voltage:
- VIN ..... -0.3 V to 62 V
- M/S ..... -0.3 V to VIN
- UVLO ..... -0.3 V to 16 V
- SW ..... -5 V to VIN
- BOOT ..... V_{SM} + 8.8 V maximum

Output voltage:
- HDRV..... V_{SM} to BOOT
- BOOT-SW, HDRV-SW (differential from BOOT or HDRV to SW) ..... -0.3 V- to 8.8 V
- VBP, LDRV, COMP, RT, ENABLE, PGOOD, SYNC ..... -0.3 V to 8.8 V
- VDD, FB, TRK, SS, ILIM ..... -0.3 V to 3.6 V

Grounding:
- AGND-PGND, PGND-AGND ..... -200 mV to 200 mV
- Power PAD to AGND (must be electrically connected external to device) ..... 0 mV

Electrostatic discharge (ESD):
- Human body model (HBM) ..... 1.0 kV
- Charged device model (CDM) ..... 1.0 kV

Junction temperature range, (T_J) ..... -55°C to +125°C

Storage temperature range, (T_{stg}) ..... -55°C to 150°C

1.4 Recommended operating conditions.

Input voltage ..... 4.5 V to 60 V

1.5 Thermal characteristics.

Thermal metric 2/	Case outline X	Units
Junction to ambient thermal resistance, θ_{JA} 3/	35.4	°C/W
Junction to case (top) thermal resistance, θ_{JCtop} 4/	38.1	
Junction to board thermal resistance, θ_{JB} 5/	10.8	
Junction to top characterization parameter, Ψ_{JT} 6/	0.5	
Junction to board characterization parameter, Ψ_{JB} 7/	10.9	
Junction to case (bottom) thermal resistance, θ_{JCbot} 8/	4.3	

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2/ For more information about traditional and new thermal metrics, see manufacturer data.

3/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K-board, as specified in JESD51-7, in an environment described in JESD51-2a.

4/ The junction to case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specified JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

5/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

6/ The junction to top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

7/ The junction to board characterization parameter, Ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

8/ The junction to case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88

2. APPLICABLE DOCUMENTS

AMERICAN NATIONAL STANDARDS INSTITUTE, SEMICONDUCTOR EQUIPMENT and MATERIALS INTERNATIONAL

ANSI SEMI STANDARD G30-88 - Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Applications for copies should be addressed to the American National Standards Institute, Semiconductor Equipment and Materials International, 1819 L Street, NW, 11 th floor, Washington, DC 20036 or online at https://www.ansi.org)

JEDEC Solid State Technology Association

JESD51	–	Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device).
JESD51-2a	–	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JESD51-8	–	Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-board
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.or online at https://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Block diagram. The block diagram shall be as shown in figure 4.

3.5.5 Simplified application. The simplified application shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
Input supply						
Input voltage range	V_{VIN}		4.5		60	V
Shutdown current	I_{SD}	V_{ENABLE} < 100 mV		1	2.5	µA
Operating current, drives not switching	I_{QQ}	V_{ENABLE} ≥ 2 V, f_{SW} = 300 kHz			4.5	mA
ENABLE						
ENABLE pin voltage to disable the device	V_{DIS}				100	mV
ENABLE pin voltage to enable the device	V_{EN}		600			
ENABLE pin source current	I_{ENABLE}				410	nA
8-V and 3.3-V regulators						
8-V regulator output voltage	V_{VBP}	V_{ENABLE} ≥ 2 V, 8.2 V < V_{VIN} ≤ 60 V, 0 mA < I_{IN} < 20 mA	7.8	8.0	8.35	V
8-V regulator dropout voltage, $V_{VIN-VVBP}$	V_{DO}	4.5 V < V_{VIN} ≤ 8.2 V, V_{EN} ≥ 2 V, I_{IN} = 10 mA		110	210	mV
3.3-V regulator output voltage	V_{VDD}	V_{ENABLE} ≥ 2 V, 8.2 V < V_{VIN} ≤ 60 V, 0 mA < I_{IN} < 5 mA	3.2	3.3	3.42	V
Fixed and programmable UVLO						
Programmable UVLO ON voltage (at UVLO pin)	V_{UVLO}	V_{ENABLE} ≥ 2 V	878	900	920	mV
Hysteresis current out of UVLO pin	I_{UVLO}	V_{ENABLE} ≥ 2 V, UVLO pin > V_{UVLO}	4.0	5	6.2	µA
VBP turnon voltage	VBP_{ON}	V_{ENABLE} ≥ 2 V, UVLO pin > V_{UVLO}	3.8		4.4	V
VBP turnoff voltage	VBP_{OFF}		3.55		4.1	
VBP UVLO Hysteresis voltage	VBP_{HYS}		175		400	mV
Reference						
Reference voltage (+ input of the error amplifier)	V_{REF}	T_J = 25°C, 4.5 V < V_{VIN} ≤ 60 V	594	600	606	mV
		-55°C ≤ T_J ≤ 125°C, .4.5 V < V_{VIN} ≤ 60 V	585	600	610	
Oscillator						
Switching frequency	f_{SW}	Range (typical)	100		600	kHz
		R_{RT} = 100 kΩ, 4.5 V < V_{VIN} ≤ 60 V	85	100	115	
		R_{RT} = 31.6 kΩ, 4.5 V < V_{VIN} ≤ 60 V	270	300	335	
		R_{RT} = 14.3 kΩ, 4.5 V < V_{VIN} ≤ 60 V	540	600	670	
Valley voltage	V_{VALLEY}		0.7	1	1.25	V
PWM gain (V_{VIN}/V_{RAMP})	K_{PWM}	4.5 V < V_{VIN} ≤ 60 V	14	15	16	V/V

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
PWM and duty cycle						
Minimum controlled pulse	$t_{ON(min)}$	$V_{VIN} \le 4.5$ V, $f_{SW} = 300$ kHz		100	160	ns
		$V_{VIN} \le 12$ V, $f_{SW} = 300$ kHz		75	130	
		$V_{VIN} \le 60$ V, $f_{SW} = 300$ kHz		50	80	
Minimum OFF time	$t_{OFF(max)}$	$V_{VIN} \le 12$ V, $f_{SW} = 300$ kHz		170	250	ns
Maximum duty cycle	D_{MAX}	$f_{SW} = 100$ kHz, $4.5 \text{ V} < V_{VIN} \le 60$ V	95%			ns
		$f_{SW} = 300$ kHz, $4.5 \text{ V} < V_{VIN} \le 60$ V	90%			
		$f_{SW} = 600$ kHz, $4.5 \text{ V} < V_{VIN} \le 60$ V	82%			
Error amplifier						
Gain bandwidth product 4/	GBWP		7	10	13	MHz
Open loop gain 4/	A_{OL}		80	90	95	dB
Input bias current	I_{IB}				135	nA
Output source current	I_{EAOP}	$V_{VFB} = 0$ V	1.8			mA
Output sink current	I_{EAOM}	$V_{VFB} = 1$ V	1.9			mA
Programmable soft start						
Soft start source current at $V_{SS} < 0.5$ V	$I_{SS(source,start)}$	$V_{SS} = 0.25$ V	42	52	62	µA
Soft start source current at $V_{SS} > 0.5$ V	$I_{SS(source,normal)}$	$V_{SS} = 1.5$ V	9.2	11.6	13.9	
Soft start sink current	$I_{SS(sink)}$	$V_{SS} = 1.5$ V	0.7	1.05	1.36	
SS pin HIGH voltage during fault (OC or thermal) reset timing	$V_{SS(fltH)}$		2.38	2.5	2.65	V
SS pin LOW voltage during fault (OC or thermal) reset timing	$V_{SS(fltL)}$		235	300	375	mV
SS pin voltage during steady state	$V_{SS(steady\_state)}$		3.2	3.3	3.55	V
Initial offset voltage from SS pin to error amplifier input	$V_{SS(offst)}$		525	650	790	mV
Tracking						
Range of TRK which overrides V_{REF}	$V_{TRK(ctrl)}$		0		600	mV

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
Synchronization (Master/Slave)						
M/S pin voltage in master mode	V_{MSTR}		3.9		VIN	V
M/S pin voltage in slave 0° mode	$V_{SLV(0)}$		1.26		1.74	V
M/S pin voltage in slave 180° mode	$V_{SLV(180)}$		0		0.74	V
SYNC pin pulldown current	$I_{SYNC(in)}$	M/S configured as slave- 0° or slave- 180°	8	11	14.5	µA
SYNC pin input high voltage level	$V_{SYNC(in\_high)}$		2			V
SYNC pin input low voltage level	$V_{SYNC(in\_low)}$				0.8	V
Minimum SYNC high pulse duration	$t_{SYNC(high\_min)}$		40			ns
Minimum SYNC low pulse duration	$t_{SYNC(low\_min)}$		40			ns
Gate drivers						
High side driver pullup resistance	R_{HDHI}	C_{LOAD} = 2.2 nF, I_{DRV} = 300 mA, T_J = -55°C to 125°C	1.37	2.64	4	Ω
High side driver pulldown resistance	R_{HDLO}		1	2.4	4	
Low side driver pullup resistance	R_{LDHI}		1.25	2.4	4	
Low side driver pulldown resistance	R_{LDLO}		0.44	1.1	1.7	
Time delay between HDRV fall and LDRV rise	$t_{NON-OVERLAP1}$	C_{LOAD} = 2.2 nF, V_{HDRV} = 2 V, V_{LDRV} = 2 V		50		ns
Time delay between HDRV rise and LDRV fall	$t_{NON-OVERLAP2}$			60		
Overcurrent protection (Low-side MOSFET sensing)						
ILIM pin source current	I_{ILIM}	4.5 V < V_{VIN} ≤ 60 V, T_J = 25°C	9	9.75	11	µA
		4.5 V < V_{VIN} ≤ 60 V, T_J = -55°C to 125°C	6.9		12	
ILIM pin source current during soft start	$I_{ILIM,(ss)}$	4.5 V < V_{VIN} ≤ 60 V, T_J = 25°C		15		
Temperature coefficient of ILIM current	$I_{ILIM, Tc}$	4.5 V < V_{VIN} ≤ 60 V		1400		ppm
ILIM pin voltage operating range	V_{ILIM}	4.5 V < V_{VIN} ≤ 60 V	50		300	mV
Overcurrent protection threshold (voltage across low-side FET for detecting overcurrent)	OCP_{TH}	R_{ILIM} = 10 kΩ, I_{ILIM} = 10 µA (V_{ILIM} = 100 mV)	-110	-100	-84	

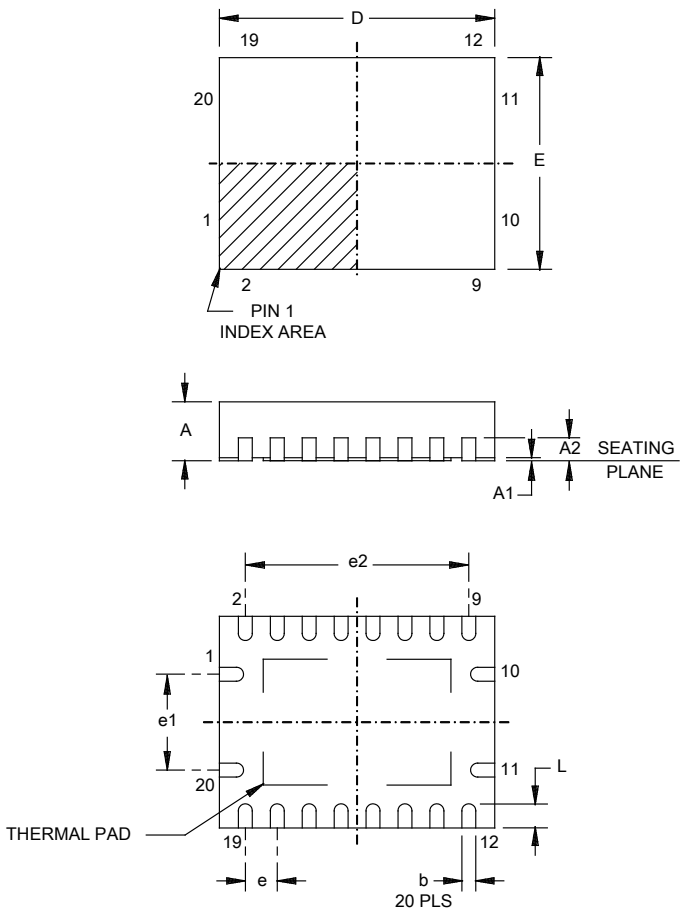
See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
Short circuit protection (High side MOSFET sensing)						
LDRV pin maximum voltage during calibration	$V_{LDRV(max)}$	R_{LDRV} = open		300	360	mV
Multiplier factor to set the SCP based on OCP level setting at the ILIM pin	A_{OC3}	R_{LDRV} = 10 kΩ	2.75	3.2	3.6	V/V
	A_{OC7}	R_{LDRV} = open	6.3	7.25	7.91	
	A_{OC15}	R_{LDRV} = 20 kΩ	13.5	16.4	18	
Thermal shutdown						
Thermal shutdown set threshold 3/	$T_{SD,set}$	4.5 V < V_{VIN} ≤ 60 V	155	165	175	°C
Thermal shutdown reset threshold 3/	$T_{SD,reset}$		125	135	145	
Thermal shutdown hysteresis	T_{hyst}			30		
Power Good						
FB pin voltage upper limit for power good	V_{OV}	4.5 V < V_{VIN} ≤ 60 V	620	647	675	mV
FB pin voltage lower limit for power good	V_{UV}		520	552	575	
Power good hysteresis voltage at FB pin	$V_{PG,HYST}$		8.4	20	33	
PGOOD pin voltage when FB pin voltage > V_{OV} or < V_{UV}, IPGD = 2 mA	$V_{PG(out)}$				100	
PGOOD pin voltage when device power is removed	$V_{PG(np)}$	V_{VIN} is open, 10-kΩ to V_{EXT} = 5 V		1	1.5	V
Boot diode						
Bootstrap diode forward voltage	V_{DFWD}	I = 20 mA	0.5	0.7	1	V
Discharge resistor from BOOT to SW	$R_{BOOT-SW}$			1		MΩ

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ These specifications apply for -55°C ≤ T_J ≤ +125°C, V_{IN} = 12 V, unless otherwise noted.
3/ Ensured by design, not production tested.
4/ Ensured by design at -40°C ≤ T_J ≤ +125°C, not production test.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.80	1.00	E	3.35	3.65
A1	0.00	0.05	e	0.50 BSC	
A2	0.20 TYP		e1	1.50 BSC	
b	0.18	0.30	e2	3.50 BSC	
D	4.35	4.65	L	0.30	0.50

NOTES:
1. All linear dimensions are in millimeters.
2. his drawing is subject to change without notice.
3. QFN (Quad Flatpack No-Lead) package configuration .
4. The package thermal pad must be soldered to the board for thermal and mechanical performance.
5. See additional figure in the manufacturer's data for details regarding the exposed thermal pad features and dimensions.
6. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
7. Falls within JEDEC MO-241 variation AB.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	ENABLE	20	UVLO
2	SYNC	19	VIN
3	M/S	18	BOOT
4	RT	17	HDRV
5	SS	16	SW
6	TRK	15	VBP
7	FB	14	LDRV
8	COMP	13	PGND
9	AGND	12	ILIM
10	VDD	11	PGOOD

FIGURE 2. Terminal connections.

Terminal		I/O	Description
Symbol	number		
AGND	9		Analog signal ground. This pin must be electrically connected to power ground PGND externally.
BOOT	18	O	Boot-capacitor node for high-side FET gate driver. The boot capacitor is connected from this pin to SW.
COMP	8	O	Output of the internal error amplifier. The feedback loop compensation network is connected from this pin to the FB pin.
ENABLE	1	I	This pin must be high for the device to be enabled. If this pin is pulled low, the device is put in a low-power- consumption shutdown mode.
FB	7	I	Negative input to the error amplifier. The output voltage is fed back to this pin through a resistor-divider network.
HDRV	17	O	Gate-driver output for the high-side FET.
ILIM	12	O	A resistor from this pin to PGND sets the overcurrent limit. This pin provides source current used for the overcurrent-protection threshold setting.
LDRV	14	O	Gate driver output for the low-side FET. Also, a resistor from this pin to PGND sets the multiplier factor to determine the short-circuit current limit. If no resistor is present, the multiplier defaults to 7 times the ILIM pin voltage
M/S	3	I	Master- or slave-mode selector pin for frequency synchronization. This pin must be tied to VIN for master mode. In the slave mode, this pin must be tied to AGND or left floating. If the pin is tied to AGND, the device synchronizes with a 180° phase shift. If the pin is left floating, the device synchronizes with a 0° phase shift
PGND	13		Power ground. This pin must externally connect to the AGND at a single point.
PGOOD	11	O	Power-good indicator. This pin is an open-drain output pin, and a 10-kΩ pullup resistor is recommended to be connected between this pin and VDD.
RT	4	I	A resistor from this pin to AGND sets the oscillator frequency. Even if operating in slave mode, it is required to have a resistor at this pin to set the free-running switching frequency.
SS	5	I	Soft-start. A capacitor must be connected from this pin to AGND. The capacitor value sets the soft-start time.

FIGURE 3. Terminal function.

Terminal		I/O	Description – Continued.
Symbol	number		
SW	16	I	This pin must connect to the switching node of the synchronous buck converter. The high-side and low-side FET current sensing are also done from this node.
SYNC	2	I/O	Synchronization. This is a bidirectional pin used for frequency synchronization. In the master mode, it is the SYNC output pin. In the slave mode, it is a SYNC input pin. If unused, this pin can be left open.
TRK	6	I	Tracking. External signal at this pin is used for output voltage tracking. This pin goes directly to the internal error amplifier as a positive reference. The lesser of the voltages between VTRK and the internal 600-mVreference sets the output voltage. If not used, this pin should be pulled up to VDD.
UVLO	20	I	Undervoltage lockout. A resistor divider on this pin from VIN to AGND can be used to set the UVLO threshold
VBP	15	O	8-V regulated output for gate driver. A ceramic capacitor with a value between 1 µF and 10 µF must be connected from this pin to PGND
VDD	10	O	3.3-V regulated output. A ceramic bypass capacitor with a value between 0.1 µF and 1 µF must be connected between this pin and the AGND pin and placed closely to this pin.
VIN	19	I	Input voltage for the controller, which is also the input voltage for the dc-dc converter. A 1-µF bypass capacitor from this pin to AGND must be added and placed closed to VIN.

FIGURE 3. Terminal function – Continued.

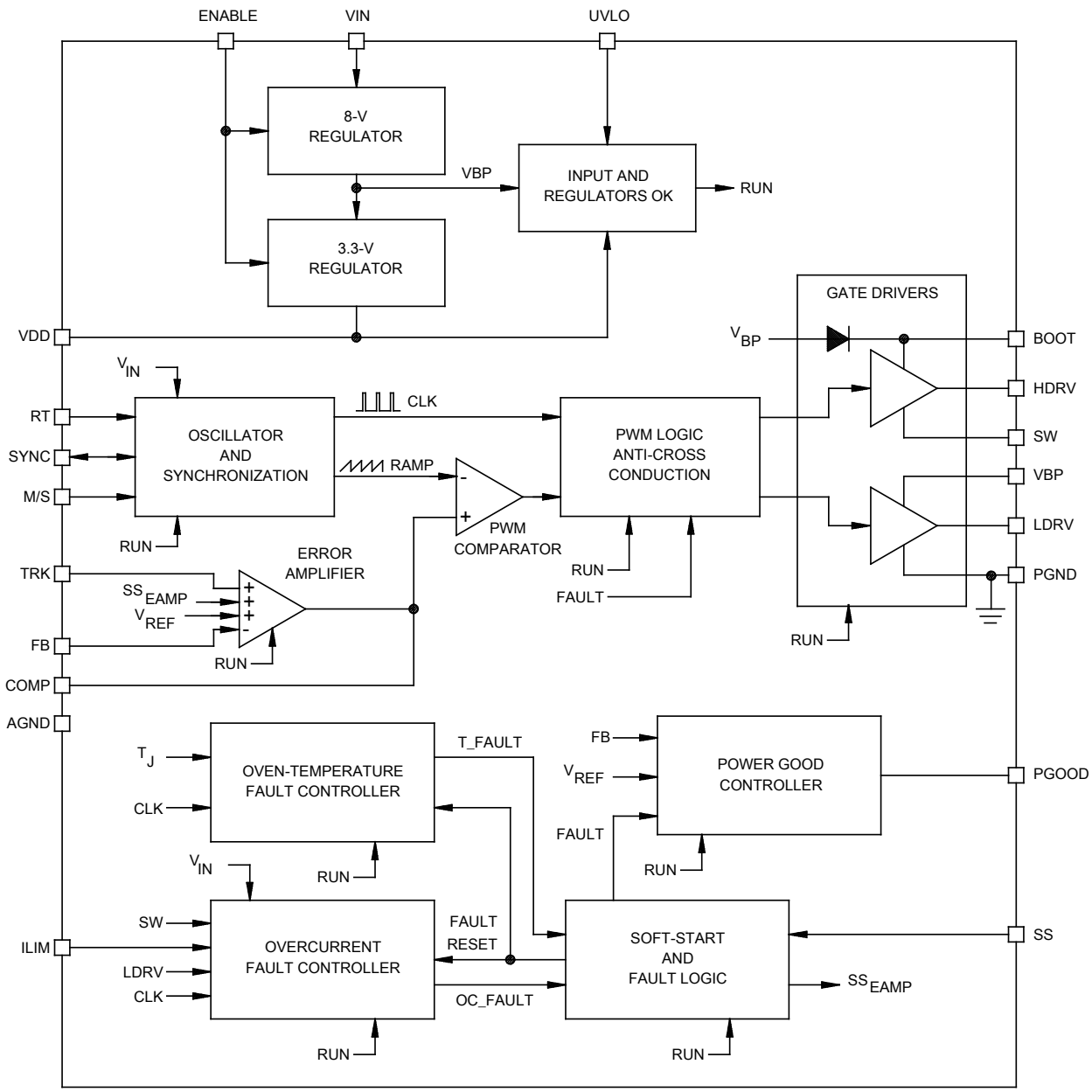


FIGURE 4. Block diagram.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/13607
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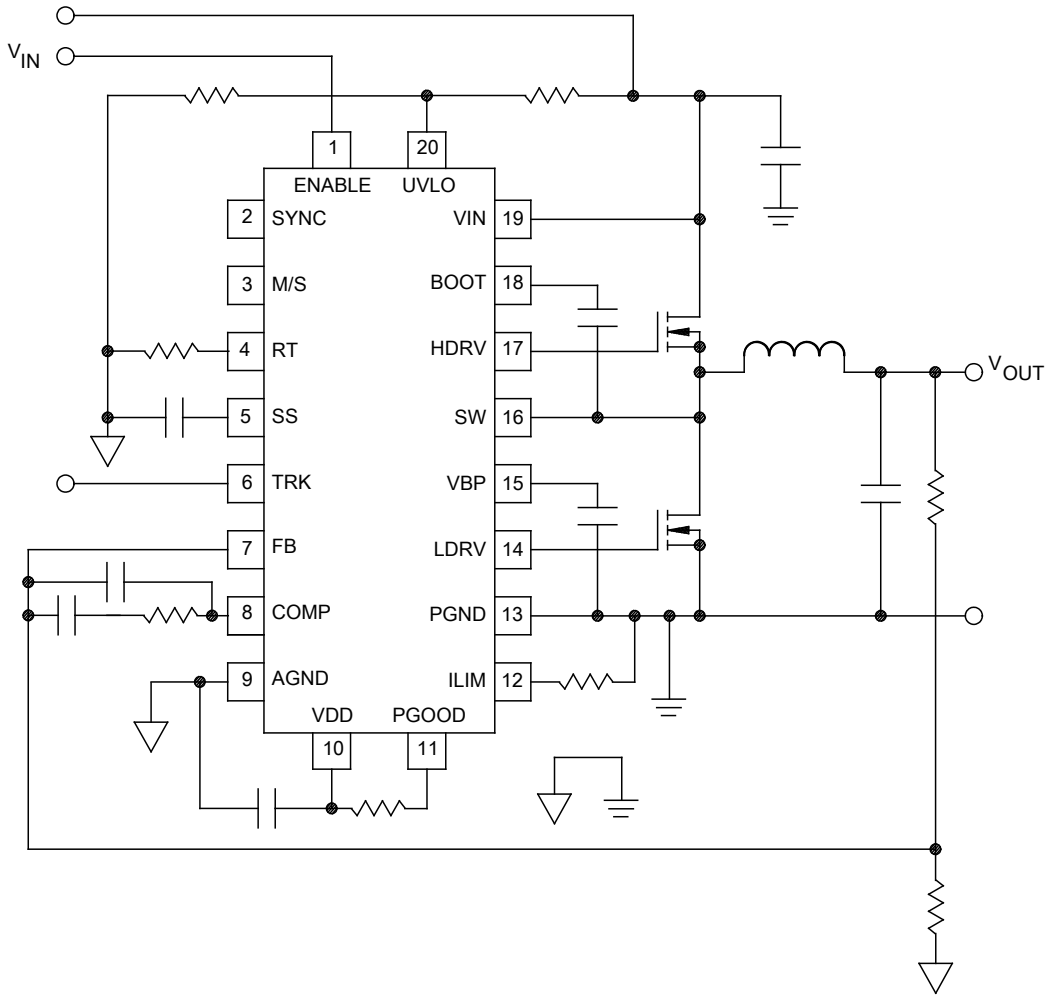

FIGURE 5. Simplified application.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/13607-01XE	01295	Tape and reel, 250 units	PZYM	TPS40170MRGYTEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243