REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to current requirements. Editorial changes throughout. - drw	04-07-14	Raymond Monnin
B	Redrawn. Update paragraphs to MIL-PRF-38535 requirements. - drw	16-08-16	Charles F. Saffle
C	Make correction to the ΔFull scale / ΔV_{SS} maximum test limit by deleting -.01 %FSR/V and replacing with +.01 %FSR/V as specified under Table I. Update document paragraphs to current MIL-PRF-38535 requirements. - ro	22-10-05	James R. Eschmeyer

Revision Status of Sheets																							
REV																							
SHEET																							
REV	C	C	C	C	C	C	C	C	C	C													
SHEET	1	2	3	4	5	6	7	8	9	10													

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

PREPARED BY
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APPROVED BY
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DRAWING APPROVAL DATE
98-10-14

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

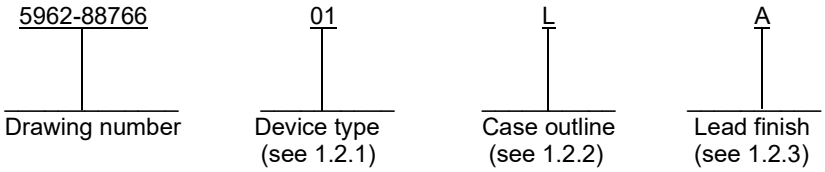
MICROCIRCUIT, DIGITAL-LINEAR, 12-BIT CMOS DIGITAL TO ANALOG CONVERTER WITH OUTPUT AMPLIFIER AND REFERENCE, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL C	SIZE A	CAGE CODE **67268**	**5962-88766**
		SHEET	1 OF 10	

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD7245A	12-Bit CMOS DAC with output amplifier and reference; parallel loading structure
02	AD7248A	12-Bit CMOS DAC with output amplifier and reference; 8+4 loading structure

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
3	CQCC1-N28	28	Square leadless chip carrier
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Positive supply voltage (V_{DD}) to AGND	-0.3 V dc to +17.0 V dc
Positive supply voltage (V_{DD}) to DGND	-0.3 V dc to +17.0 V dc
V_{DD} to V_{SS}	-0.3 V dc to +34.0 V dc
AGND to DGND	-0.3 V dc to V_{DD}
Digital input voltage to DGND	-0.3 V dc to V_{DD} + 0.3 V dc
V_{OUT} to AGND	V_{SS} to V_{DD}
V_{OUT} to V_{SS}	0 V dc to +24.0 V dc
V_{OUT} to V_{DD}	-32 V to 0 V dc
Voltage reference output (REF OUT) to AGND	0 V to V_{DD}
Power dissipation to +75°C 2/	450 mW
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C

1/ Stresses above absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Above +75°C, derate at a factor of 6 mW/°C.

1.4 Recommended operating conditions.

Single supply:

Positive supply voltage (V_{DD})	+15 V ±5%
Negative supply voltage (V_{SS})	0 V
AGND = DGND	0 V

Dual supply:

Positive supply voltage (V_{DD})	+12 V to +15 V ±5%
Negative supply voltage (V_{SS})	-12 V to -15 V ±5%
AGND = DGND	0 V
Load resistance (R_L)	2 kΩ to GND
Load capacitance (C_L)	100 pF to GND
REF OUT	Unloaded
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution	RES		1, 2, 3	All		12	Bits
Relative accuracy	RA	V_{DD} = +11.4 V to +15.75 V V_{SS} = -11.4 V to -15.75 V	1, 2, 3	All	-1	+1	LSB
Differential nonlinearity	DNL	Guaranteed monotonic	1, 2, 3	All	-1	+1	LSB
Unipolar offset error	UOE	V_{SS} = 0 V or -11.4 V to -15.75 V	1, 2, 3	All	-5	+5	LSB
DAC gain error 2/	GE		1, 2, 3	All	-2	+2	LSB
Full scale output 3/	V_{OUTE}	V_{DD} = +15 V	1	All	-.2	+.2	%FSR
voltage error			2, 3		-.6	+.6	
ΔFull scale / ΔV_{DD}		V_{DD} = +10.8 V to +16.5 V	1	All	-.06	+.06	%FSR/V
ΔFull scale / ΔV_{SS}		V_{SS} = -10.8 V to -16.5 V	1	All	-.01	+.01	%FSR/V
Reference output	V_{REFOUT}	V_{DD} = +15 V, V_{SS} = -15 V	1	All	4.99	5.01	V
ΔReference / ΔV_{DD}		V_{DD} = +10.8 V to +16.5 V	1	All		2	mV/V
Reference load sensitivity		Reference load current change (0 - 100 μA). Not including R_{OFS} current.	1, 2, 3	All	-1.0	+1.0	mV
Digital input high voltage	V_{INH}		1, 2, 3	All	2.4		V
Digital input low voltage	V_{INL}		1, 2, 3	All		0.8	V
Digital input current 4/ for data and control inputs	I_{IN}	V_{IN} = 0 or V_{DD}	1, 2, 3	All	-10	+10	μA
Digital input capacitance	C_{IN}	see 4.3.1b	4 5/	All		8	pF
Output range resistors	R_{OUT}		1, 2, 3	All	15	30	Ω
Output ranges 6/		Pin strappable	1, 2, 3	All	0	5	V
		Minimum load resistance			0	10	
		2 k to GND			-5	+5	
Power supply current	I_{DD}	Output unloaded	1, 2, 3	All		12	mA
	I_{SS}					5	
Functional tests		see 4.3.1c	7, 8	All			
Output voltage settling 7/ positive and negative full scale change	t_{SL}	To $\pm$0.5 LSB, R_L = 2 kΩ, see 4.3.1b	4 5/	All		10	μs
Output voltage slew rate	SR	See 4.3.1b	4, 5, 6 5/	All	1.5		V/μs

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip select pulse width	t_1		9, 10, 11	All	100		ns
Write pulse width	t_2		9, 10, 11	All	100		ns
Chip select to write setup	t_3		9, 10, 11	All	0		ns
Chip select to write hold	t_4		9, 10, 11	All	0		ns
Data valid to write setup time	t_5		9, 10, 11	All	80		ns
Data valid to write hold time	t_6		9, 10, 11	All	10		ns
Load DAC pulse width	t_7		9, 10, 11	All	100		ns
Clear pulse width	t_8		9, 10, 11	01	100		ns

1/ Dual supply: V_{DD} = 11.4 V to 15.75 V, V_{SS} = 0 V or -11.4 V to -15.75 V, AGND = DGND = 0 V, R_L = 2 kΩ to GND, C_L = 100 pF to GND. REF unloaded, unless otherwise stated.

2/ This error is calculated with respect to the reference voltage and is measured after the offset error has been allowed for.

3/ This error is calculated with respect to an ideal 4.9988 V (on the 5 V range) or 9.9976 V (on the 10 V range). Typical full scale temperature coefficient is ±30 ppm of FSSR/°C.

4/ Control inputs are $\overline{CS}$, $\overline{WR}$, $\overline{LDAC}$ and $\overline{CLR}$ for device 01 and $\overline{CSMSB}$, $\overline{CSLSB}$, $\overline{WR}$ and $\overline{LDAC}$ for device 02.

5/ Subgroups 4, 5 and 6 shall be measured only for initial test, or after process or design changes which may affect the parameter in those subgroups.

6/ 0 to +10 applies to V_{DD} = +15 V ±5% only, and V_{SS} = -15 V ±5%.

7/ For positive full scale change, DAC register loaded all 0's to all 1's. For negative full scale change, DAC register loaded all 1's to all 0's.

Device types	01		02
Case outlines	3	L	R
Terminal number	Terminal symbol		
1	NC	V_{SS}	V_{SS}
2	V_{SS}	R_{OFS}	R_{OFS}
3	R_{OFS}	REF OUT	REF OUT
4	REF OUT	AGND	AGND
5	AGND	DB11	(MSB) DB7
6	DB11	DB10	DB6
7	DB10	DB9	DB5
8	NC	DB8	DB4
9	DB9	DB7	DB3
10	DB8	DB6	DGND
11	DB7	DB5	DB2
12	DB6	DGND	DB1
13	DB5	DB4	(LSB) DB0
14	DGND	DB3	$\overline{CSMSB}$
15	NC	DB2	$\overline{CSLSB}$
16	DB4	DB1	$\overline{WR}$
17	DB3	DB0	$\overline{LDAC}$
18	DB2	$\overline{CS}$	V_{DD}
19	DB1	$\overline{WR}$	R_{FB}
20	DB0	$\overline{LDAC}$	V_{OUT}
21	$\overline{CS}$	$\overline{CLR}$	
22	NC	V_{DD}	
23	$\overline{WR}$	R_{FB}	
24	$\overline{LDAC}$	V_{OUT}	
25	$\overline{CLR}$		
26	V_{DD}		
27	R_{FB}		
28	V_{OUT}		

FIGURE 1. Terminal connections.

Device type 01

$\overline{CLR}$	$\overline{LDAC}$	$\overline{WR}$	$\overline{CS}$	Function
H	L	L	L	Both latches are transparent
H	H	H	X	Both latches are latched
H	H	X	H	Both latches are latched
H	H	L	L	Input latches are transparent
H	H	_Γ	L	Input latches are latched
H	L	H	H	DAC latches are transparent
H	_Γ	H	H	DAC latches are latched
L	X	X	X	DAC latches loaded with all 0's
_Γ	H	H	H	DAC latches loaded with all 0's and output remains at 0 V or -5 V
_Γ	L	L	L	Both latches are transparent and output follows input data

H = High state L = Low state X = Don't care

Device type 02

$\overline{CSLSB}$	$\overline{CSMSB}$	$\overline{WR}$	$\overline{LDAC}$	Function
L	H	L	H	Loads LS byte into input latch
L	H	_Γ	H	Latches LS byte into input latch
_Γ	H	L	H	Latches LS byte into input latch
H	L	L	H	Loads MS nibble into input latch
H	L	_Γ	H	Latches MS nibble into input latch
H	_Γ	L	H	Latches MS nibble into input latch
H	H	H	L	Loads input latch into DAC latch
H	H	H	_Γ	Latches input latch into DAC latch
H	L	L	L	Loads MS nibble into input latch and Loads input latch into DAC latch
H	H	H	H	No data transfer operation

H = High state L = Low state X = Don't care

FIGURE 2. Truth tables.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 4, 5, and 6 shall be measured only for the initial test and after process or design changes which may affect the specified parameters in those subgroups.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 22-10-05

Approved sources of supply for SMD 5962-88766 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-88766013A	24355	AD7245ATE/883B
5962-8876601LA	24355	AD7245ATQ/883B
5962-8876602RA	3/	AD7248ATQ/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland