



How approach a heavy ions test on a new device technology using SiC power devices as an example.

Radiation Test Workshop – 2016 April 1st

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How approach a heavy ions test on a new device technology using SiC power devices as an example.



HV SiC Schottky Diodes Testing

- SiC Schottky Diodes degradation under heavy ions
 - Problem Description
- Test Approach:
 - Not well understood phenomenon
 - Safe Operating Area to be defined
- Dependency of degradation with LET and Bias: Phases definition and execution
 - Phase 1: Critical LET and Bias allocation
 - Phase 2: Degradation evaluation
 - Phase 3: Safe Operating Area verification

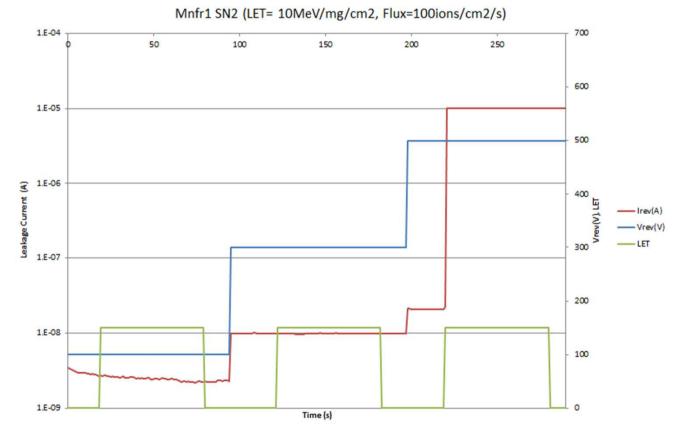
SiC Power MOSFET Testing

• Test Results Summary

Heavy Ions Testing of HV SiC Schottky Diodes Problem Description



Problem description: Dramatic increase of Irev of SiC Schottky Diodes observed for devices from the main SiC manufacturers while HV biasing under heavy ions radiation



Heavy lons Testing of HV SiC Schottky Diodes Test Approach



Test Approach:

- Not well understood phenomenon
 - Test outcome could be helpful for manufacturers to improve the devices resistance to heavy ions
 - Geometry
 - Quality of the raw material: Wafer, epi...
- Not a PASS/FAIL radiation test:
 - Devices are going to fail but, we want to extract the maximum information possible about the failure. Need of flexibility because a rough initial approach can lead to 0 information
- Safe operating ranges still to be defined
 - Dependency of degradation with LET and Bias has to be studied in order to delimit a safe operation area of the devices. Sensitivity exists but derating enough the devices can be an option for a lot of applications.

This leads to a Several Phases Test Approach

Heavy Ions Testing of HV SiC Schottky Diodes Test Approach



Test Approach:

- Test Phases Definition
 - Phase 1: Critical LET and Bias values allocation
 - Has to be performed for each part type under test
 - Phase 2: Degradation characterization:
 - Critical test parameters found during phase 1 give an idea of when the degradation starts to occur. Testing around that level allows to quantify the effect
 - Annealing effect study
 - Phase 3: Safe Operating Area verification
 - Testing the devices in an operating area near but under the parameter thresholds found during Phases 1 and 2.
 - If no degradation appears for a high fluence at that combination of parameters we can define a safe area.
 - LET of interest (depending on final application) shall be focused and define which is the maximum voltage the device withstands without degrading under heavy ions

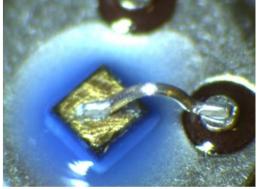
Heavy Ions Testing of HV SiC Schottky Diodes Samples Preparation

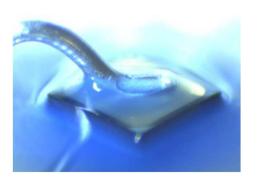


Samples preparation:

- Removal of silicone coatings when present in order to allow the heavy ions to reach the active area of the devices
- Parylene coating of 15µm in order to avoid arcing during high voltage testing under heavy ions







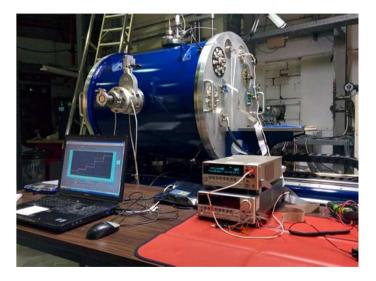
- Functional test of the devices after silicone removal
 - Problems in spare parts without silicone at high voltage (900V)
 - No issues after parylene coating. All the devices are stable and can be tested up to the proposed reverse bias values

Heavy lons Testing of HV SiC Schottky Diodes Test Setup and Facilities

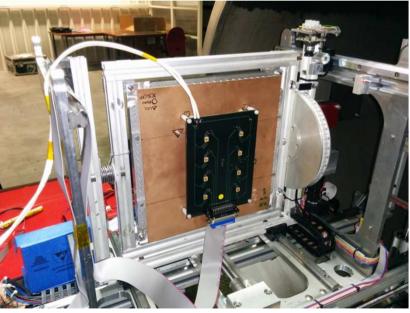


General Considerations

- Several phases approach needs more beam time but aims to obtain more accurate results
- Minimize beam time (test cost) maximizing number of DUT in test board.
 - Reduces the number of openings of the vacuum test chamber.
- Ion type changes shall also be minimized



UCL Heavy lons Radiation Facilities with monitoring test setup



Test board designed to allow HV biasing and 4w intermediate measurements of up to 8 devices

Heavy Ions Testing of HV SiC Schottky Diodes Phase 1 Description



Phase 1: Allocation of critical Reverse Voltage for each LET

• Dramatic failures resulting in damaged devices but...

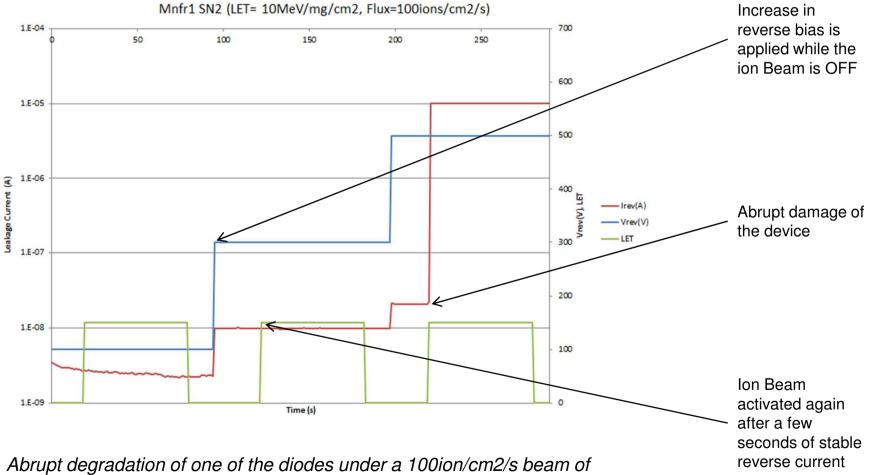
• Information on which voltages use in phase 2.

Fixed LET		Bias Steps (wide range)		MNFR	Part type	Maximum rated reverse voltage (V	Bias In Pro	s Steps itially posed
↓ Fresh device for next LET		Irev Monitoring		Α	1	1200	100, 300,	500, 700, 900
				Α	2	650	100, 200,	300, 400, 500
				Α	3	600	100, 200,	300, 400, 500
TIEXLET				В	4	250	50, 100, ⁻	150, 200, 250
			С	5	1200	100, 300, 500, 700, 900		
Also tests with DUT tilted were performed in order change LET but					lon	Tilting (º)	LET MeV/mg /cm2	
					²² Ne ⁷⁺	0	3	
SEE Cross Section decreases with						⁴⁰ Ar ¹²⁺	0	10.1
angle (already observed in Si)					⁵⁸ Ni ¹⁸⁺	0	20.4	
					⁸³ Kr ²⁵⁺	0	32.6	

Heavy lons Testing of HV SiC Schottky Diodes Phase 1 Execution



Phase 1: Execution



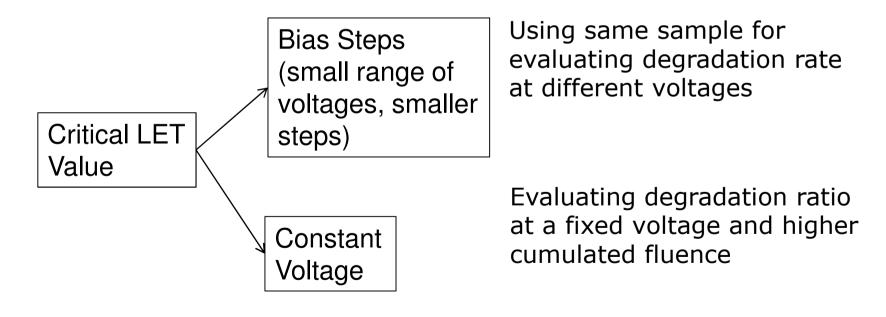
10MeV/mg/cm2 just after activating the beam during the 700V bias step. The reverse leakage is setup limited to 10uA.

Heavy Ions Testing of HV SiC Schottky Diodes Phase 2 Description



Phase 2: Degradation characterization

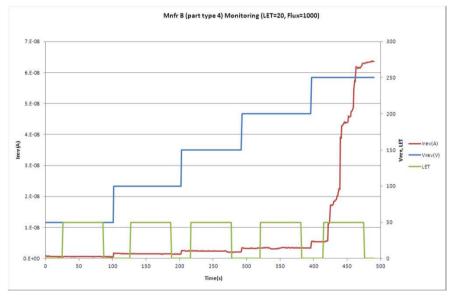
- Bias levels adjusted using info collected during phase 1
 - Progressive degradation of the device is observed
 - This allows evaluation of the Irev increase ratio Vs:
 - Bias Voltage
 - Flux of the beam



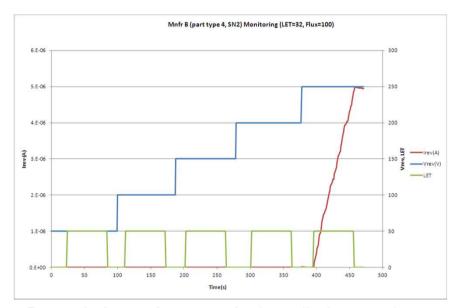
Heavy Ions Testing of HV SiC Schottky Diodes Phase 2 Execution



Phase 2: Execution



Degradation of one of the diodes under a 1000ion/cm2/s beam of 20.4MeV/mg/cm2 after a few seconds maintaining 250V reverse bias. The reverse leakage is setup increases constantly while the device stays under radiation.

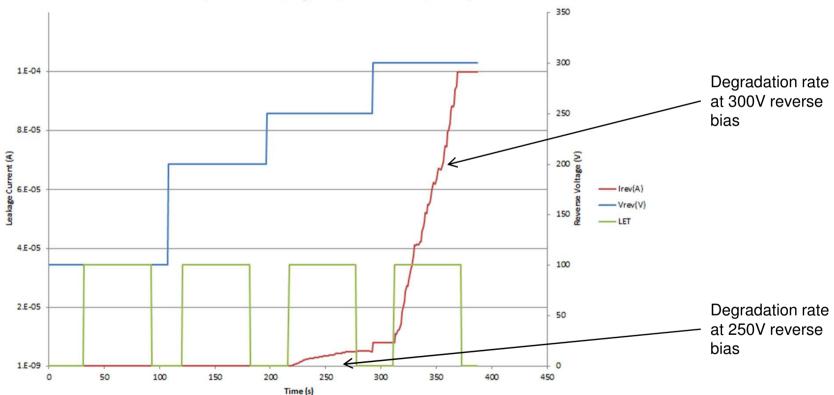


Degradation of one of the diodes under a 100ion/cm2/s beam of 32.6MeV/mg/cm2 starts immediately after applying 250V reverse bias. The reverse leakage is setup increases constantly while the device stays under radiation. This degradation is much higher than the one observed with a LET=20.4MeV/mg/cm2

Heavy lons Testing of HV SiC Schottky Diodes Phase 2 Execution



Phase 2: Execution



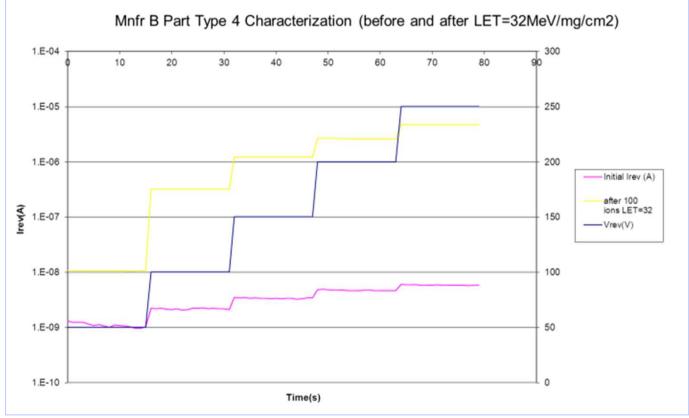
SN5 (LET=32.6MeV/mg/cm2, Flux=100ions/cm2/s)

Monitoring of one of the devices under heavy ions with an LET of 32.6MeV/mg/cm2 and a Flux of 100part/s/cm2. Increase of 50V in reverse bias (from 250 to 300V) increases degradation rate by around 20 times

Heavy Ions Testing of HV SiC Schottky Diodes Phase 2 Execution



Phase 2: Execution



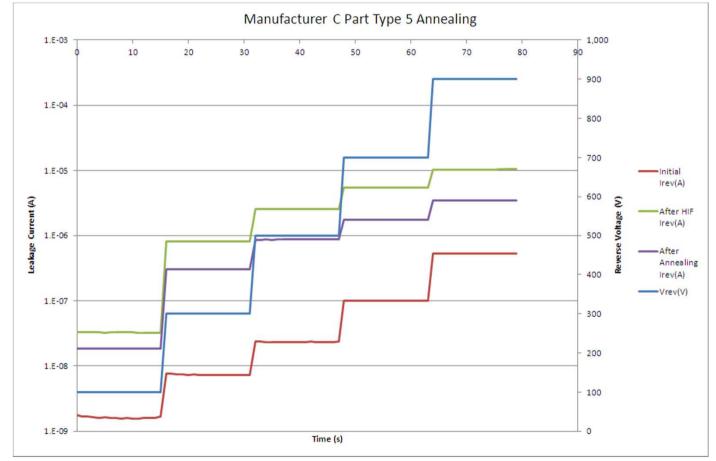
Initial and final reverse characterization of one of the devices before and after the heavy ions test with a LET of 32.6MeV/mg/cm2 and a Flux of 100part/s/cm2. The degraded device shows an increase in the reverse leakage although remains functional and stable.

Heavy lons Testing of HV SiC Schottky Diodes Phase 2 Execution



Phase 2: Execution

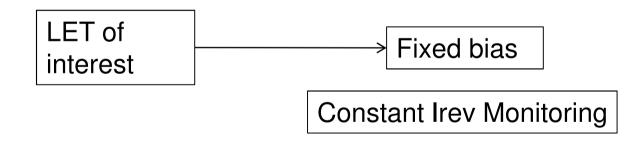
Annealing evaluation: Slight improvement after high temperature annealing (12h, 200°C, nitrogen atmosphere)





Phase 3: Safe Operation Range definition

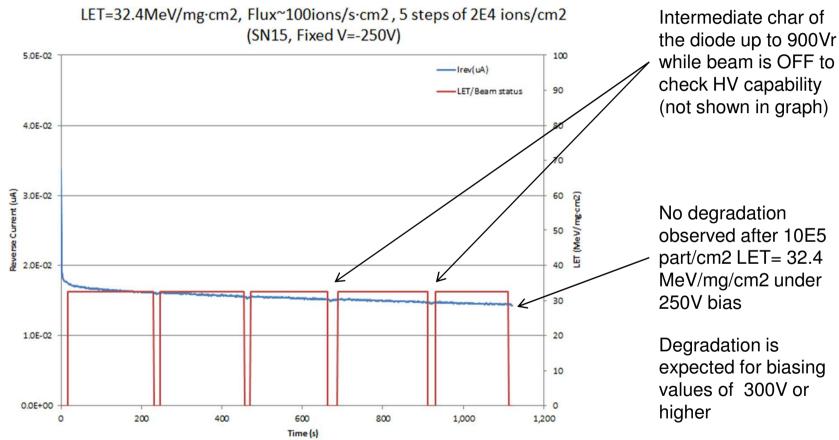
- Bias levels adjusted using info collected during phases 1 & 2
 - Allocate maximum voltage with no degradation for a certain LET level of interest. Lower LETs than that will imply higher secure maximum voltages



Heavy Ions Testing of HV SiC Schottky Diodes Phase 3 Execution



Phase 3: Safe Operation Range definition



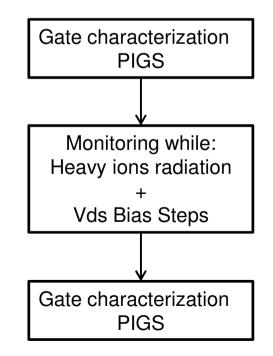
Maximum rated voltage for this device is 1200V but under heavy ions radiation... only 250V or less is safe



- SiC Power MOSFET Heavy Ions Testing Summary
- Radiation Campaign performed onto two part types
 - Initial Test Approach
 - Drain Bias and Id monitoring -> No info
 - Intermediate characterization of the devices -> No info
 - -> Only Latent Gate degradation revealed during PIGS

Test Conditions used:

- Vds in steps up to 200V with Id monitoring
- Vgs = 0V, (-1V in some samples)
- Intermediate gate characterization after each radiation step
- Combinations of:
 - LET up to 80MeV/mg/cm2
 - Flux up to 1000part/cm2/s
- Facilities: UCL (Belgium)



Heavy Ions Testing of SiC Power MOSFET - Results Summary



SiC MOSFET under heavy ions radiation:

Part Type	SN	LET (MeV/mg/cm²)	Flux (part/cm²/s)	Vgs (V)	Vds (V, 1min per step)	Results
MOSFET Manufacturer 3	SN2	3.3 (¹⁵ N ³⁺ , 0⁰)	100	0	50-100-150-200	ok
	SN3	15.9 (⁴⁰ Ar ⁸⁺ , 0⁰)	100	0	50-100-150-200	slight gate degradation
	SN4	20.4 (⁴⁰ Ar ⁸⁺ , 39 ^o)	50	0	50-100-150-200	ok
		20.4 (⁴⁰ Ar ⁸⁺ , 39 ^o)	50	-1	50-100-150-200	ok
		20.4 (⁴⁰ Ar ⁸⁺ , 39 ^o)	200	0	50-100-150-200	gate degradation
		20.4 (⁴⁰ Ar ⁸⁺ , 39º)	100	0	50-100-150-200	gate degradation
	SN5	18.1 (⁴⁰ Ar ⁸⁺ , 29º)	50	0	50-100-150-200	gate degradation
Σ	SN3		gate degradation			
	SN2	8.0 (²⁰ Ne ⁴⁺ , 37⁰)	50	0	50-100-150-200	ok
		8.0 (²⁰ Ne ⁴⁺ , 37 ^o)	200	0	50-100-150-200	ok
		8.0 (²⁰ Ne ⁴⁺ , 37⁰)	100	0	50-100-150-200	ok
MOSFET Manufacturer 4	SN1	3.3 (¹⁵ N ³⁺ , 0⁰)	100	0	50-100-150-200	ok
	SN2	15.9 (⁴⁰ Ar ⁸⁺ , 0⁰)	100	0	50-100-150-200	ok
		15.9 (⁴⁰ Ar ⁸⁺ , 0º)	200	0	50-100-150-200	ok
		15.9 (⁴⁰ Ar ⁸⁺ , 0⁰)	1000	0	50-100-150-200	ok
	SN3	20.4 (⁴⁰ Ar ⁸⁺ , 39º)	50	0	50-100-150-200	gate degradation
	SN4	18.1 (⁴⁰ Ar ⁸⁺ , 29º)	50	0	50-100-150-200	ok
		18.1 (⁴⁰ Ar ⁸⁺ , 29º)	50	-1	50-100-150-200	ok
		18.1 (⁴⁰ Ar ⁸⁺ , 29⁰)	200	0	50-100-150-200	ok
		18.1 (⁴⁰ Ar ⁸⁺ , 29º)	200	-1	50-100-150-200	gate degradation

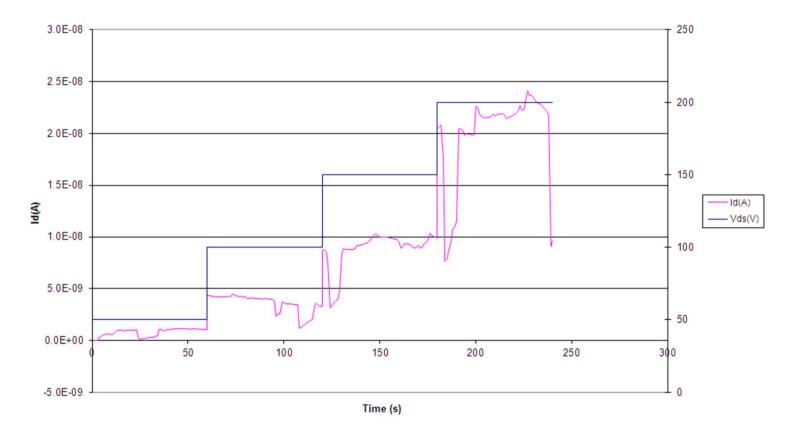
Review of technical activities - Results: Heavy Ions Radiation



SiC MOSFET under heavy ions radiation:

• Stable drain current during radiation steps

Drain current monitoring during irradiation (LET=3.3MeV/mg/cm2, FLUX=100part/cm2/s)

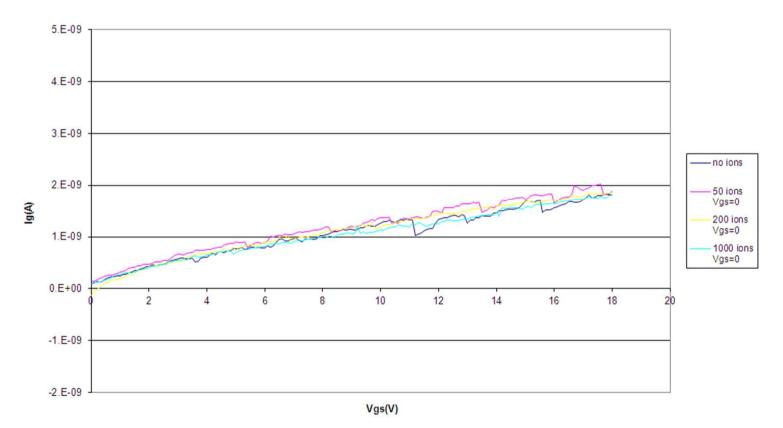


Review of technical activities - Results: Heavy Ions Radiation



SiC MOSFET under heavy ions radiation:

• No gate degradation after low LET radiation (using different fluxes)



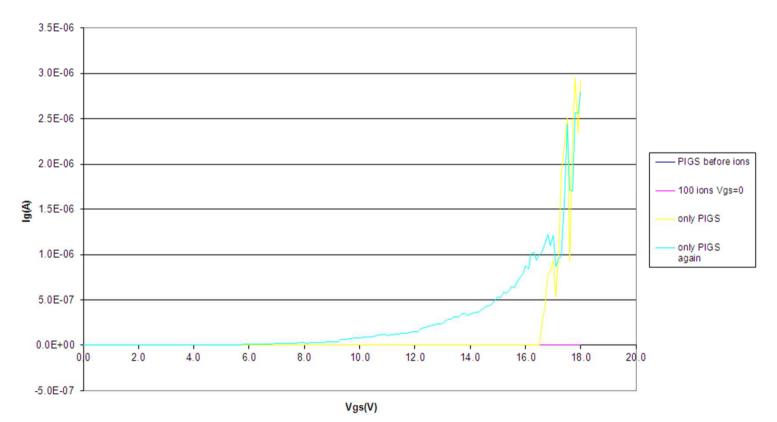
PIGS SN28.0MeV

Review of technical activities - Results: Heavy Ions Radiation



SiC MOSFET under heavy ions radiation:

 Degradation observed during PIGS after radiation steps with LET>8MeV/mg/cm2



PIGS SN3 15.9MeV (Several PIGS)

Review of technical activities Conclusions



SiC MOSFET under heavy ions radiation:

- MOSFET study Conclusions:
 - Only latent SEGR was observed in this study:
 - -> Higher Vgs during irradiation shall be used to observe in-test SEGR
 - No SEB was observed in this study but bibliography points that should be observed:

-> Higher Vds biasing is needed and HV precautions shall be taken (i.e. parylene coating)

Ongoing project: Radiation Hardening of SiC MOS

- Different gate geometries
- Different oxide types
- Several Vgs will be used to observe in-test SEGR

-> Output will be an improved gate geometry + optimized gate oxide (taking also into account TID results...)



Thank you for your attention **Contact: Juan Moreno** Juan.moreno@altertechnology.com