Radiation test strategies for a manufacturer using third party dice

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3D plus
a HEICO company

Outline

- Third party dice radiation test for manufacturer
- The new radiation test challenge and 3D PLUS solution
- Future Radiation test strategy – design oriented strategy

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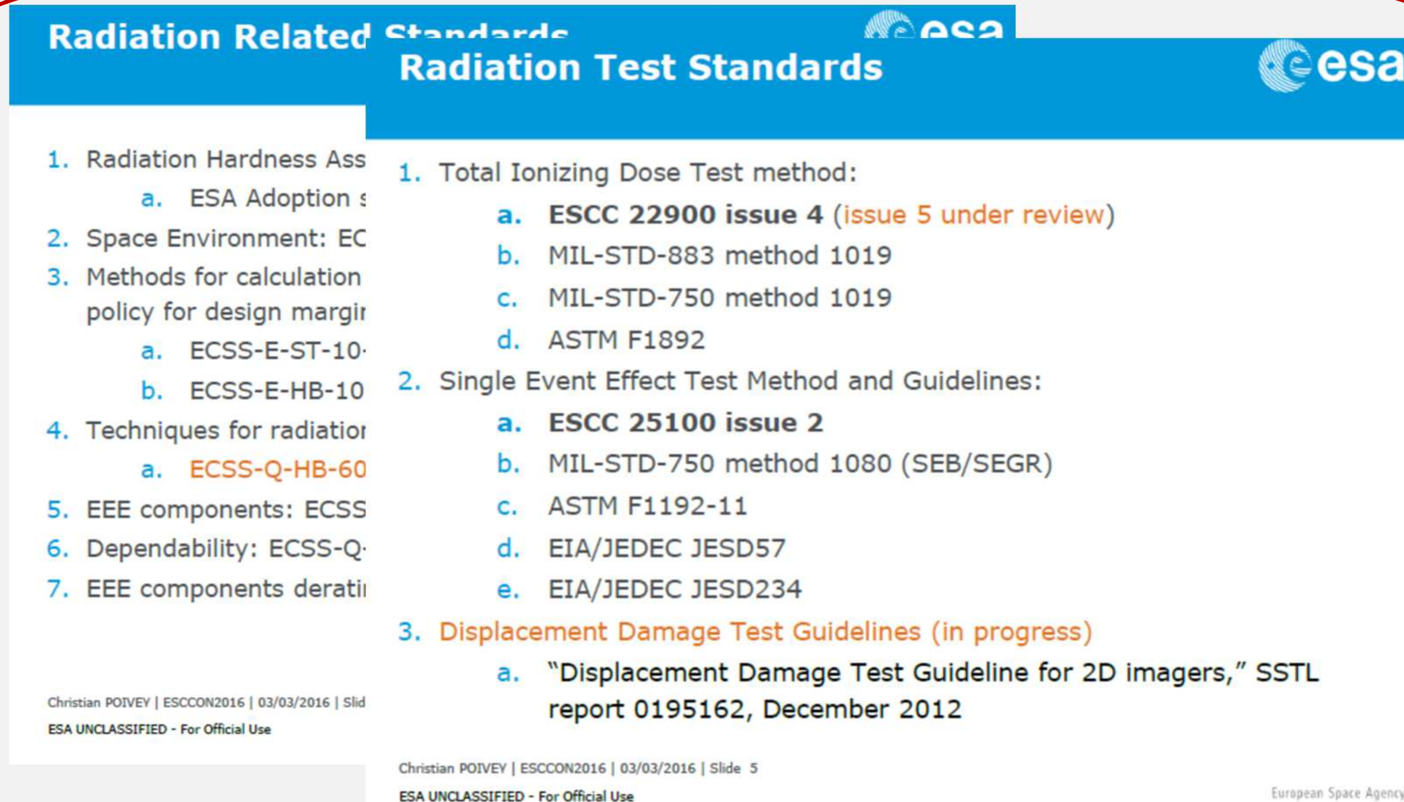
Radiation test ~~strategies~~ for a manufacturer using third party dice



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The difficulties without the strategy

Radiation test ~~strategies~~ for a manufacturer using third party dice

- The General background is that the space market volume is negligible comparing to commercial market – no bargaining power;
- What ever RH die or COTs, the detail designs are always treated as confidential by semiconductor – mostly cases are like the black box;
- Sometimes it is difficult to get general process information (ex: bipolar? CMOS? bulk? epi?...), and most time it is impossible to get detail process information (ex: gate oxide, isolation structure details…) – hard to estimate the radiation characteristics;
- It is very difficult to get the full traceability from commercial vendors – to guarantee what we tested and what we will use;

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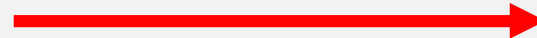
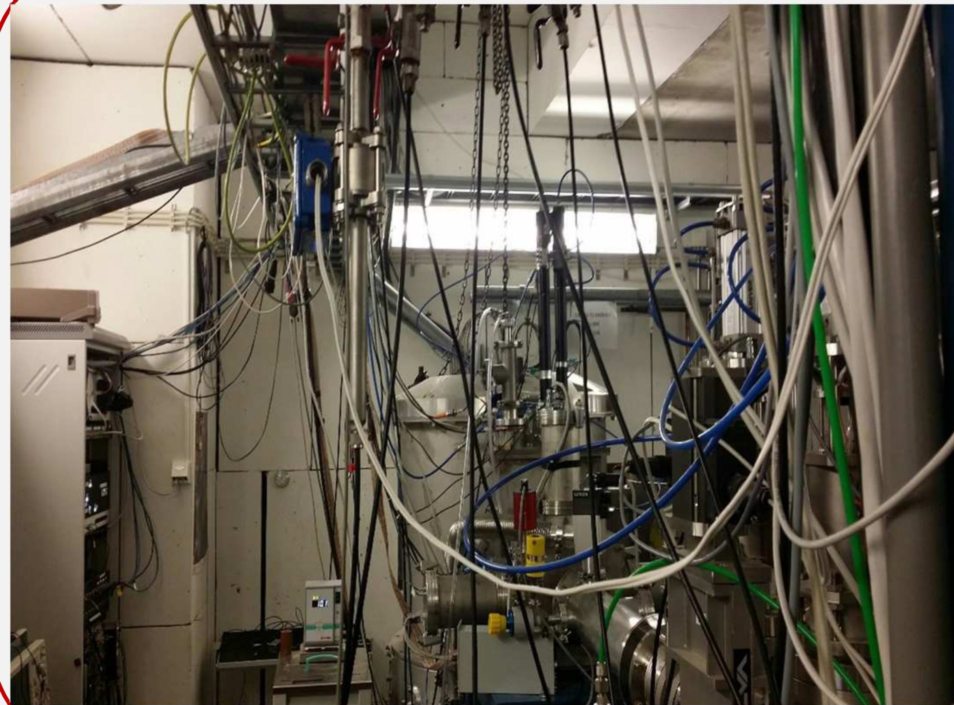
Radiation test ~~strategies~~ for a manufacturer using third party dice

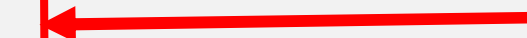
Exigent



Designer



Market



Pressure

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When the space comes into high scaling Deep submicron (DSM) semiconductors, new technical & commercial challenges show up:

Technically, DSM radiation behavior is complicated to manage:

- New structure & process are not always good to radiation;
- Big variations from process to process, manufacturer to manufacturer, design to design, revision to revision, P/N to P/N, lot to lot and even now piece to piece;
- Hard error mix with soft error: bit flip from TID; Micro Latch up (High current SEFI) & SEL, permanent SEFI
- Complicated Soft errors: single bit error, double bit error, multi-bit error, row error, column error, stuck bit, persistent flip bit & annealing, temporary SEFI, persistent SEFI, device SEFI, high current event…

Commercially, Semiconductors optimize their manufacturing to lower the cost, but it is sometimes catastrophe to space:

- Shrinking the process, modifying the materials, changing the foundry
- Shorter life cycle: 6 months to 1 year life cycle comparing 1 to 2 years component qualification
- Semiconductor Product Long Life Management (PLM) is highly risky to space traceability
- Combining Die design makes die mask verification difficult (MLC & SLC)

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A Evaluation/Qualification, Stocking, and Reuse system has been established at 3D PLUS to manage third party dice radiation test

- A fairly large evaluations when looking for the candidate (ex: around 20 SRAMs had been scanned)
- Make the completely qualification (following ECSS/ESCC standard) when a potential good die shows up
- Make a strategic inventory (bargaining power) at 3D PLUS to make sure traceability and technical supports
- Reuse the result and do further design oriented tests to put more added values

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Evaluate and Select the suitable memory die ex: Flash/DRAM

- Radiation Errors
  - Hard Errors
    - TID
    - SEL
  - Soft Errors
    - SEU
    - SEFI

Guaranteed by qualification

Guaranteed by Mitigation

3D PLUS Module
+
RHBD Controller

3D PLUS solution: Hi-Rel Electronics combining Space Radiation Harden by Design (RHBD) and Commercial Off –The-Shelf (COTS) performance to meet mission's requirements

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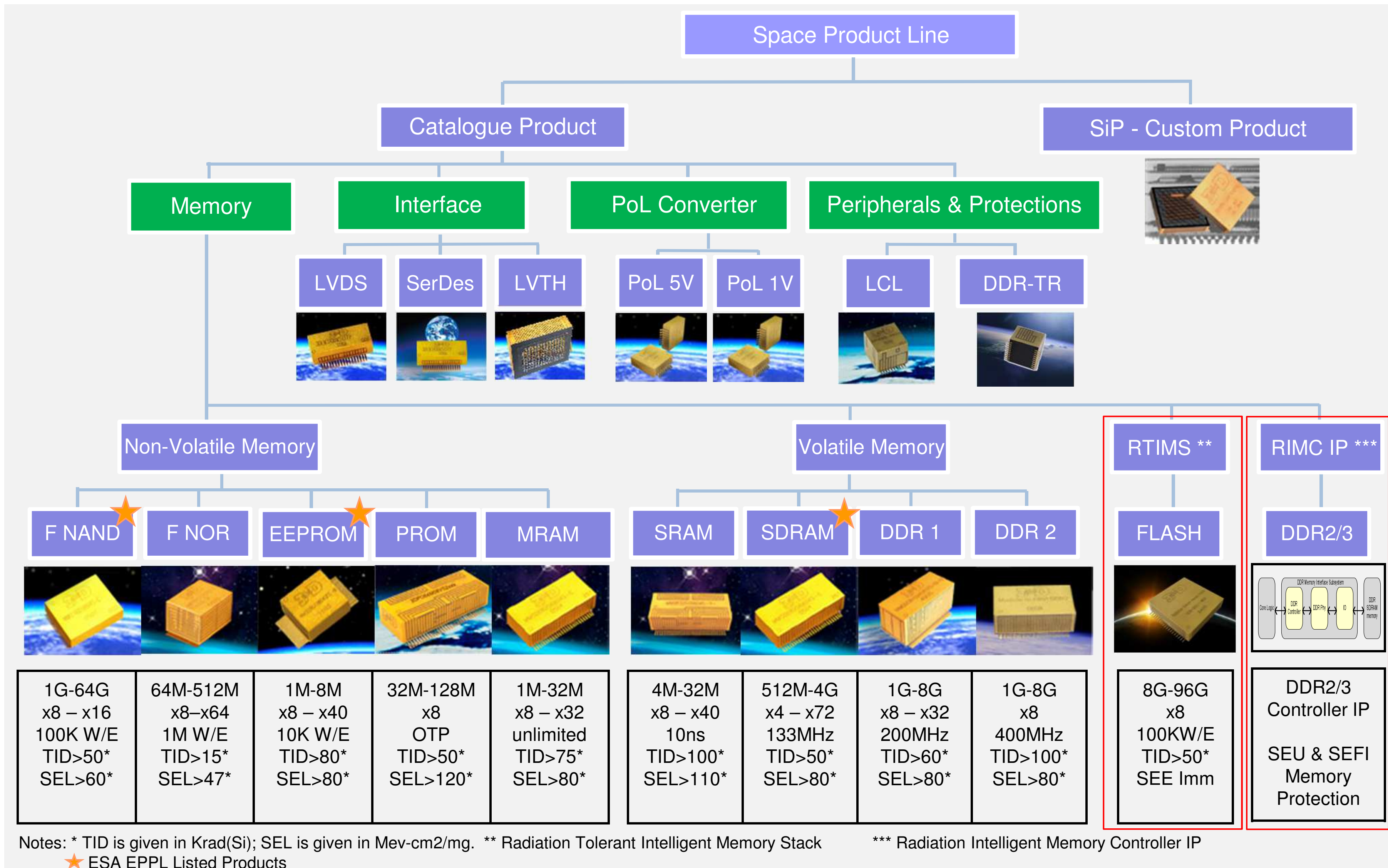
Space Products Portfolio



F NAND	F NOR	EEPROM	PROM	MRAM	SRAM	SDRAM	DDR 1	DDR 2	FLASH	DDR2/3
1G-64G x8 – x16 100K W/E TID>50* SEL>60*	64M-512M x8–x64 1M W/E TID>15* SEL>47*	1M-8M x8 – x40 10K W/E TID>80* SEL>80*	32M-128M x8 OTP TID>50* SEL>120*	1M-32M x8 – x32 unlimited TID>75* SEL>80*	4M-32M x8 – x40 10ns TID>100* SEL>110*	512M-4G x4 – x72 133MHz TID>50* SEL>80*	1G-8G x8 – x32 200MHz TID>60* SEL>80*	1G-8G x8 400MHz TID>100* SEL>80*	8G-96G x8 100KW/E TID>50* SEE Imm	DDR2/3 Controller IP SEU & SEFI Memory Protection

Notes: * TID is given in Krad(Si); SEL is given in Mev-cm2/mg. ** Radiation Tolerant Intelligent Memory Stack *** Radiation Intelligent Memory Controller IP

★ ESA EPPL Listed Products

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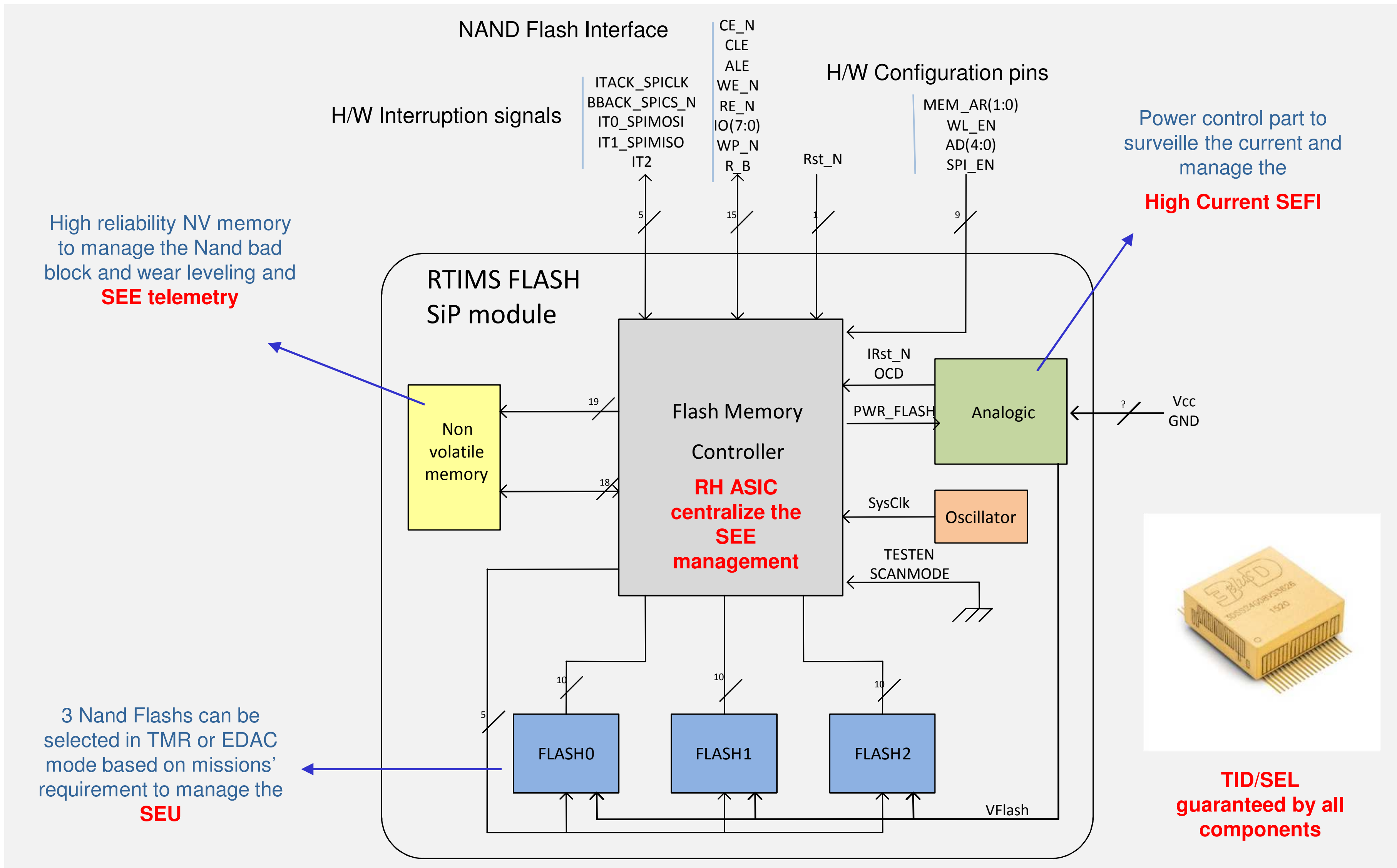

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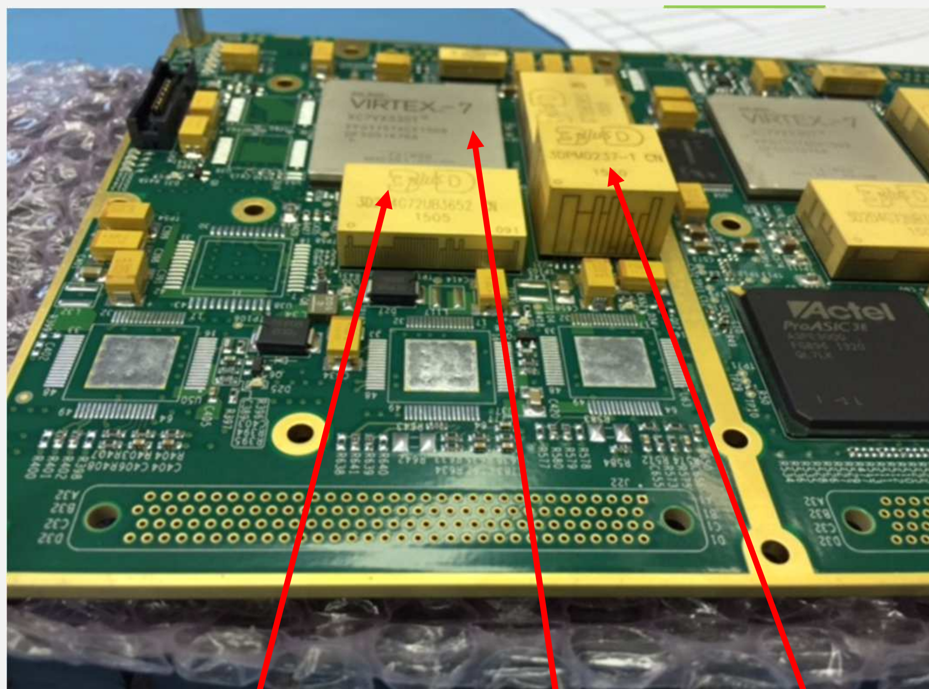
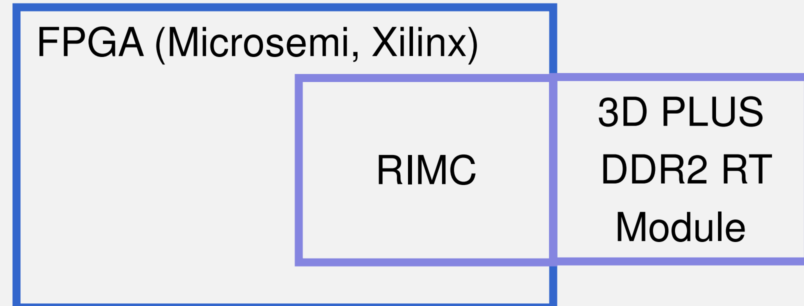
RIMC IP – RH DDR2/3 Solution





now

Memory Module + Controller IP core + DDR2 TR = Full plug & play RH DDR2 memory Solution

- The IP Controller enables a consistent and fully validated DDR2/3 Memory system solution
- The user: no need to test the DDR2/3 memory, understand the radiation behavior, design the radiation mitigation algorithm, qualify or demonstrate the system performance
- The designer: focus on the application code development

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3D PLUS radiation test strategies to use third party dice:

- Following ECSS/ESCC standard to do the radiation test
- Maintain a privilage relationship with semiconductors
- More added value tests oriented to design (radiation mitigation)

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