



Radiation Test Workshop 2016

TID characterization of Rad-Hardened 1.2GHz PLL IP from new ST CMOS 65nm space technology



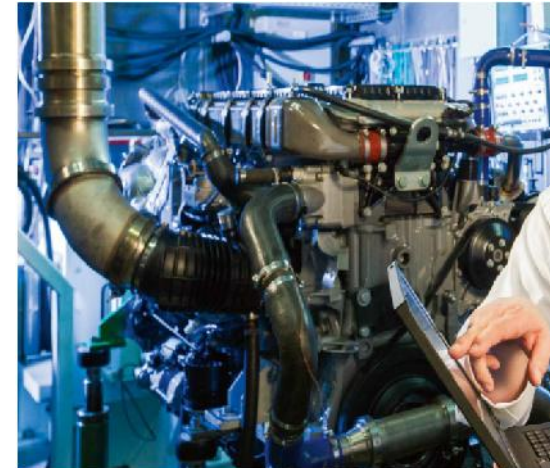
Florence Malou (CNES), Gilles Gasiot (STM), Dimitri Soussan (STM),
Philippe Roche (STM), Pierre Fontana (HRX), Frédéric Tilhac (HRX)



ENERGY



IT



MOBILITY



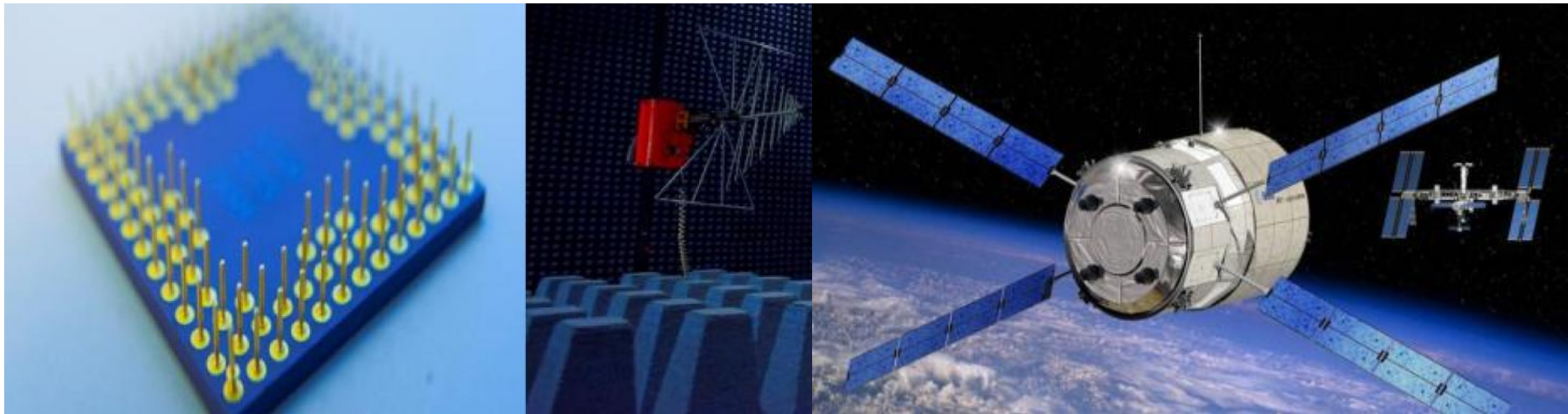
HEALTH AND NUTRITION



NATURAL RESOURCES



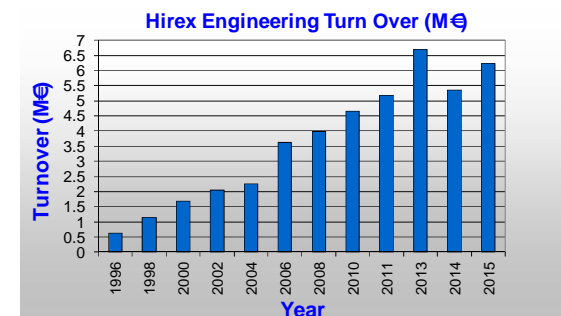
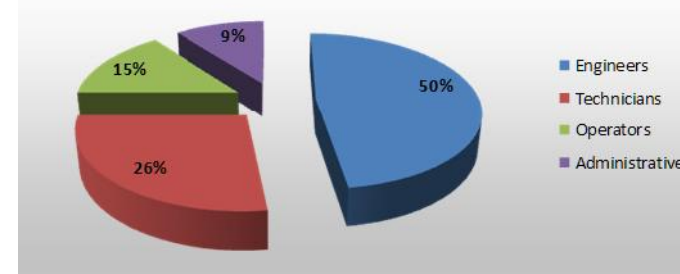
AEROSPACE & ELECTRONIC



Alter technology group: with **30** years experience in the sector.



- Hirex Engineering founded in January 1993.
- Hirex Engineering joined ALTER Technology Group in January 2007.
 - ATN based in Madrid, Seville, Roma, Portsmouth and Shanghai.
 - ATN employees 230 as of today.
 - ATN Turn-over 65 M€.
- 100% Privately owned by TÜV NORD since 29th June 2011.
- Hirex Engineering :
 - Based in Toulouse.
 - 48 employees as of today.
 - 1800 m² Facility.
 - Certified ISO 9001, EN 9100 and ISO 14001.



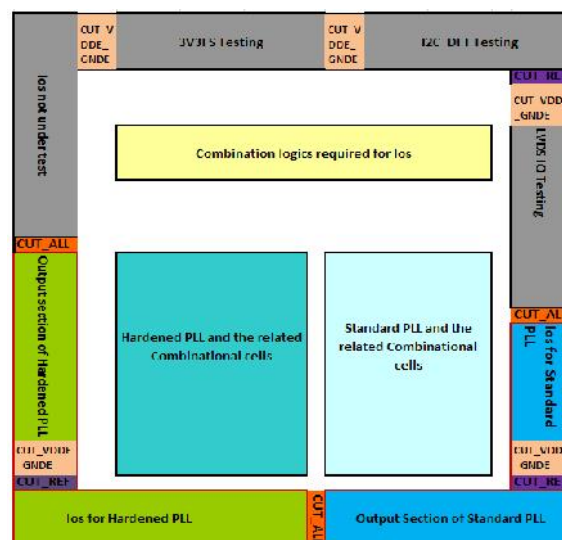
PIRADVAL Analog test-chip blocks

➤ Space design and technology platform derived from a commercial CMOS 65 nm including hardened library:

- Standard cells library.
- Memories compilers.
- Cold-spare IO.
- 1.2 GHz PLL.

➤ PIRADVAL Analog test-chip main blocks :

- Rad-Hardened PLL (PLL1201).
- Standard PLL.
- Hardened Bidirectional IO :
 - IO65LPHVT @ 1.8V
 - IO65LPHVT @ 2.5V
 - IO65LPHVT @ 3.3V
- Hardened I2C :
 - IO65LPHVT @ 1.8V
 - IO65LPHVT @ 2.5V
 - IO65LPHVT @ 3.3V
- Hardened LVDS IO.
 - IO65LPHVT @ 2.5V
 - IO65LPHVT @ 3.3V
- Cold spare LVDS IO embedded @ 2.5V up to 650Mbps.



PIRADVAL test-chip block diagram

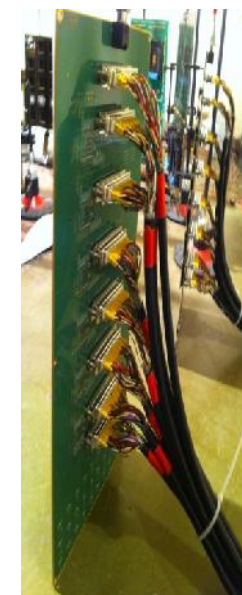
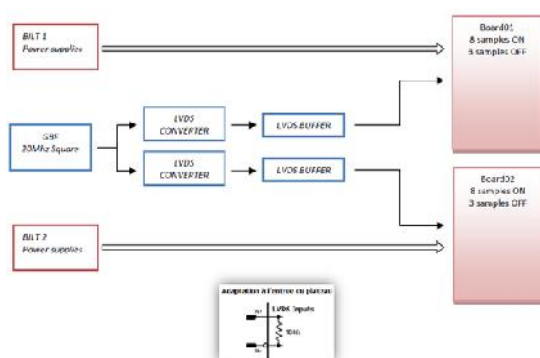


PIRADVAL test-chip layout

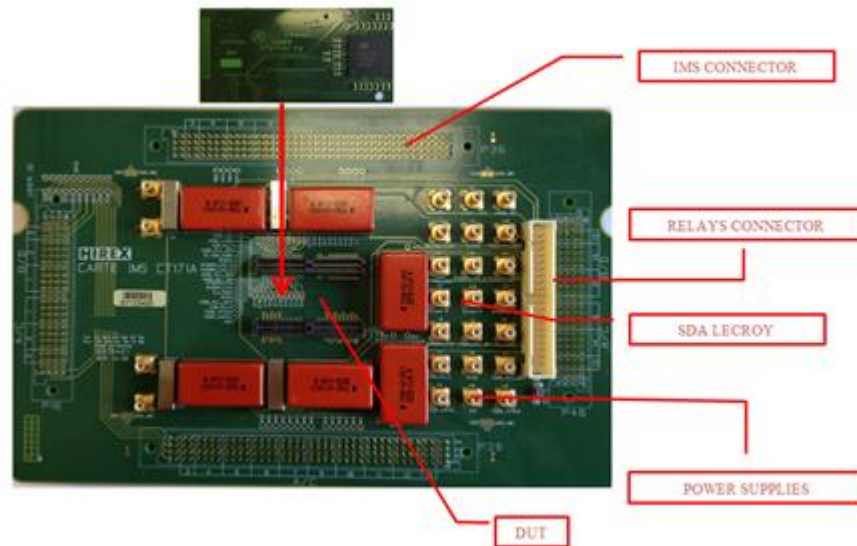
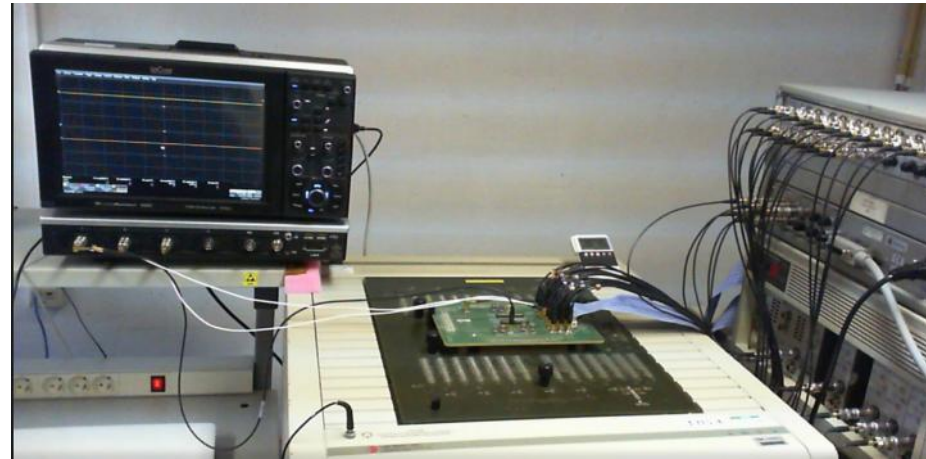
PIRADVAL TID test campaigns

- 2 x TID test campaigns have been performed :
 - First TID test campaign specific focused on Rad-Hard, standard PLLs and cold sparing.
 - Second TID test campaign specific focused on IO types, Supply voltages and cold sparing.

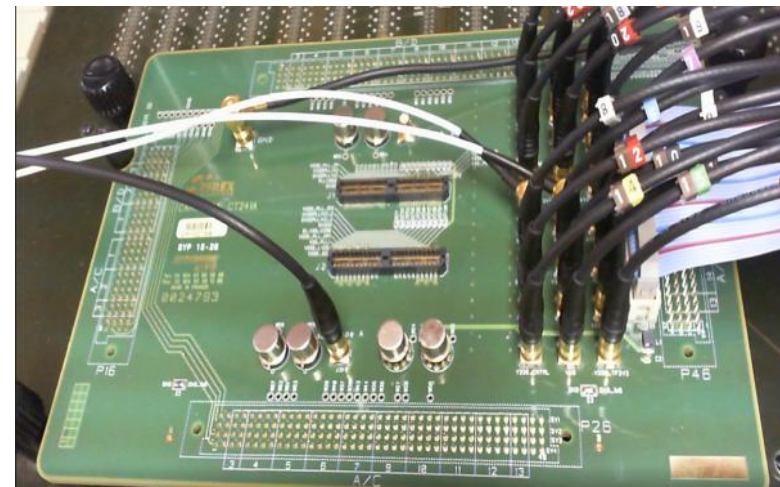
- TID testing performed at UCL:
 - According to ESCC22900 test method.
 - Dose rate 200rad(Si)/hour.
 - Radiation level : 300 krads (Si) covering the needs of Telecommunication missions.
 - 2 x times 22 devices (16 devices biased ON, 6 devices biased OFF) from 2 diffusion lots.
 - 25°C anneal under bias during 24 hours was performed followed by an accelerated ageing under bias at 100°C during 168 hours.
 - All along exposure and annealing, **84 supply currents** (42 supplies / lot) were continuously monitored



PIRADVAL test setup



1st TID campaign test setup

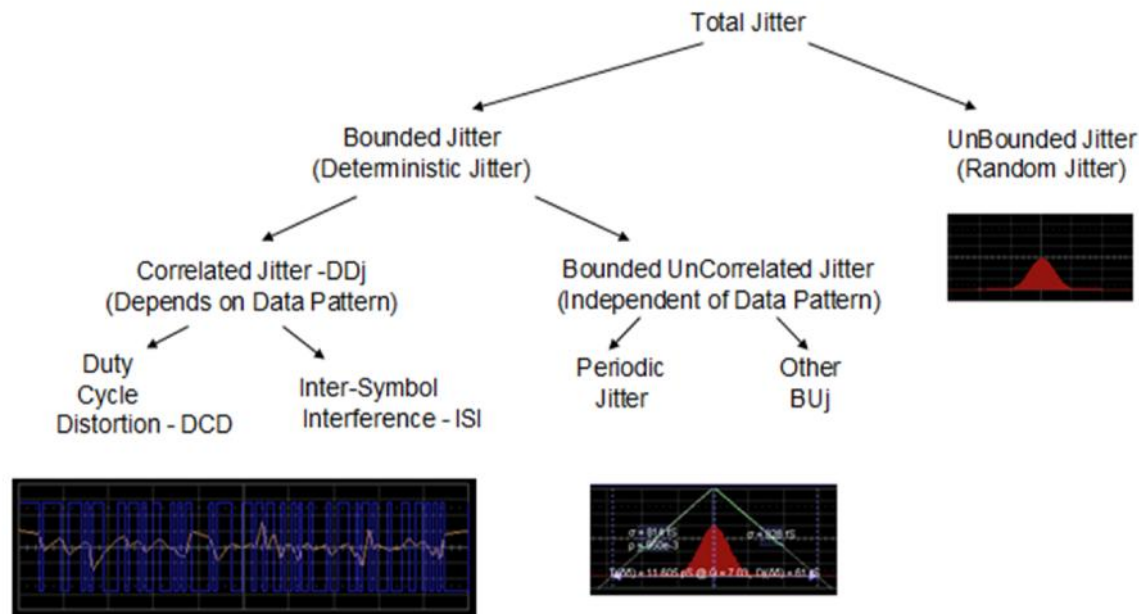


2nd TID campaign test setup

PLL measurements

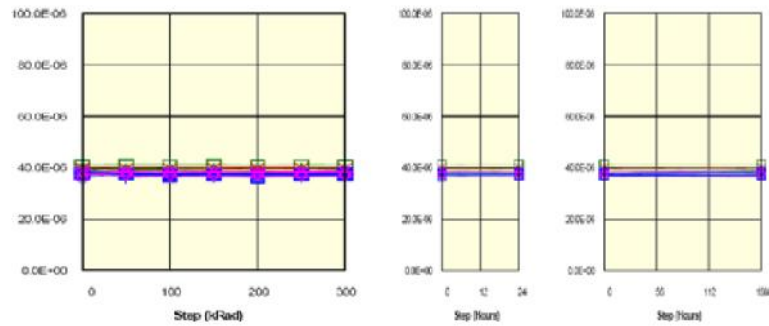
Jitter definitions

- Deterministic jitter : Includes all timing variations that are bounded in nature.
- Two types of deterministic jitter :
 - Data dependent jitter (DDj) : Results from waveform distortion and consists of intersymbol interference.
 - Bounded uncorrelated Jitter (BUj) : Comes from outside interference such as clock leakage, power supply noise, EMI and crosstalk. Much of this jitter is periodic nature and can be measured in the jitter spectrum.
 - Periodic jitter : Is any harmonic jitter source that is not sourced from the data signal itself.

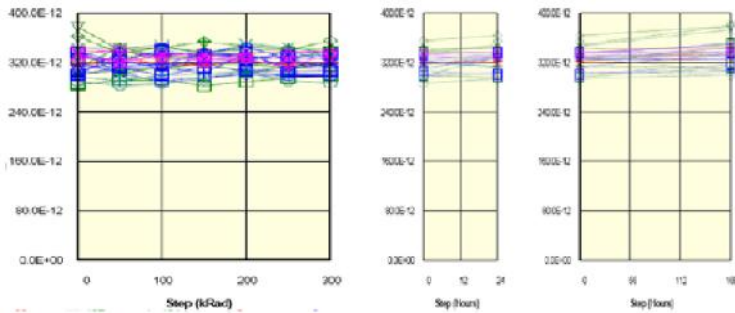


PLLs measurements

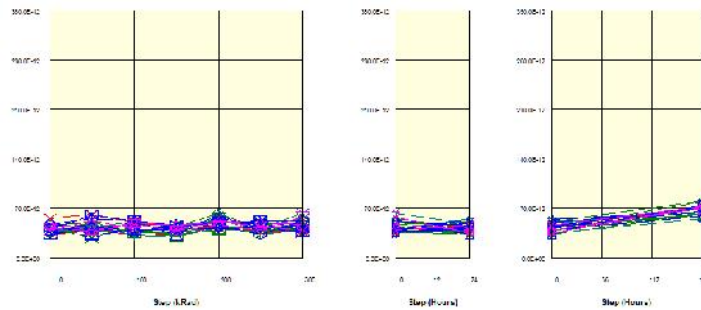
Comparison: Rad-Hard vs Std



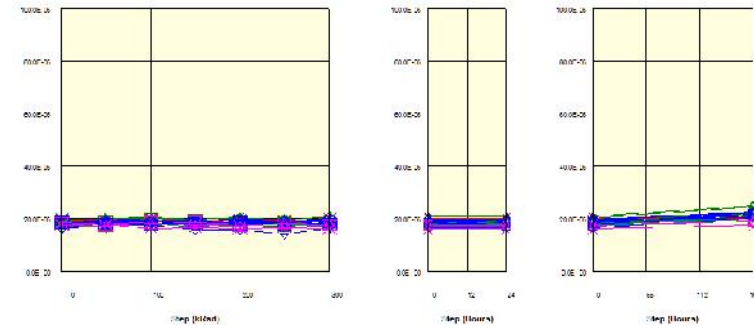
Rad-Hard PLL Lock time versus TID (unit in second)



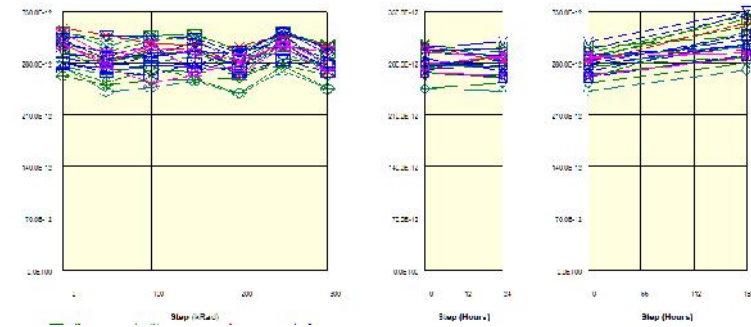
Rad-Hard PLL Total Jitter versus TID (unit in second)



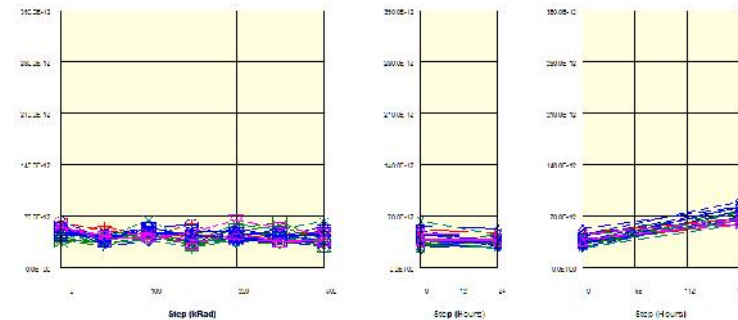
Rad-Hard PLL Periodic Jitter versus TID (unit in second)



Standard PLL Lock time versus TID (unit in second)

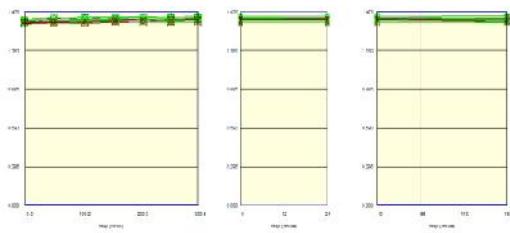


Standard PLL Total Jitter versus TID (unit in second)

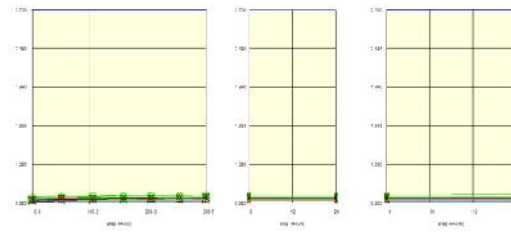


Standard PLL Periodic Jitter versus TID (unit in second)

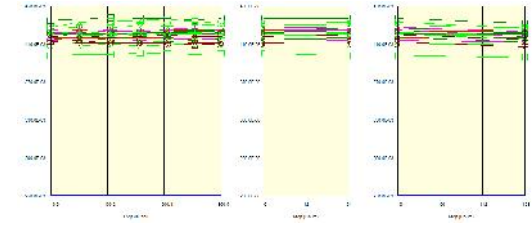
IOs Characterization Results (IOs and LVDS IOs)



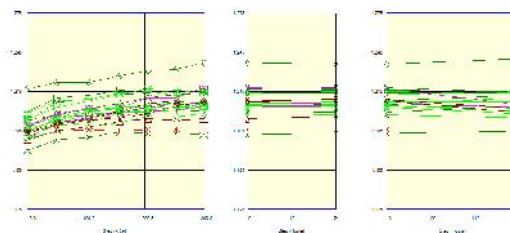
VOH versus TID (unit in volt)



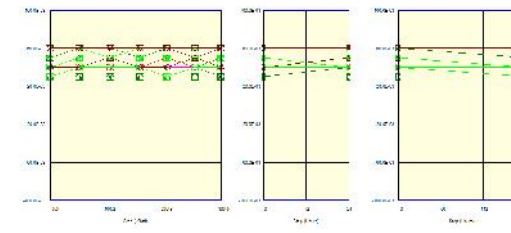
VOL versus TID (unit in volt)



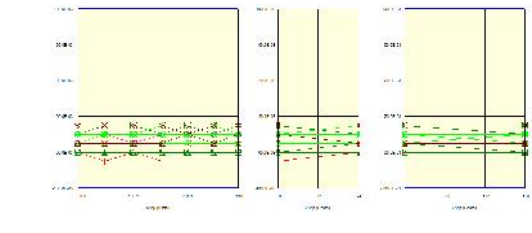
Output differential voltage VOD
versus TID (unit in volt)



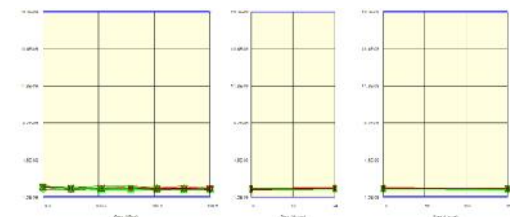
Output Offset voltage Vcm_VOS
versus TID (unit in volt)



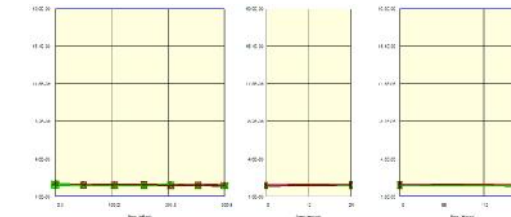
Input differential voltage high Vth
versus TID (unit in volt)



Input differential voltage low Vtl
versus TID (unit in volt)



Propagation Delay Low to High tpLH
Versus TID (unit in second)

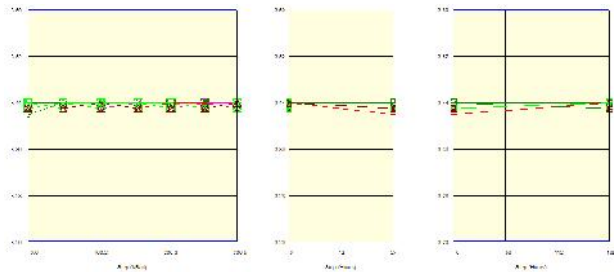


Propagation Delay High to Low tpHL
Versus TID (unit in second)

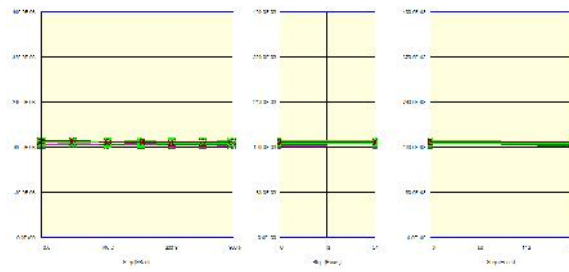


Skew tpLHA - tpHLB
Versus TID (unit in second)

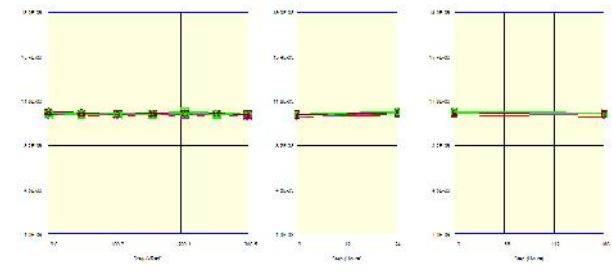
IOs Characterization Results (BIDIR)



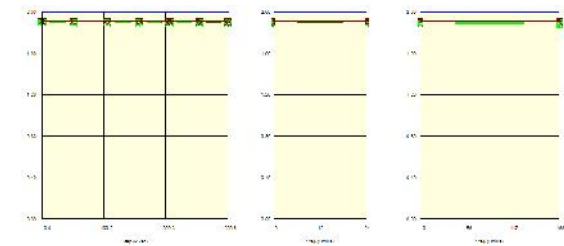
VOH BIDIR versus TID (unit in volt)



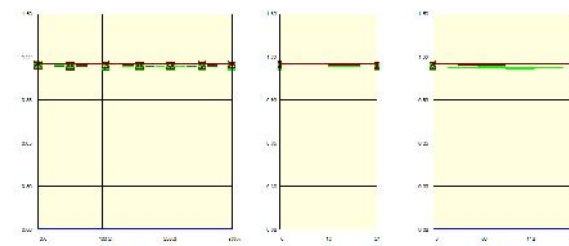
VOL BIDIR versus TID (unit in volt)



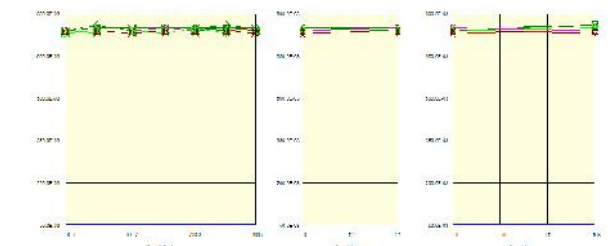
Propagation Delay HIOs BIDIR Versus TID (unit in second)



VIH BIDIR versus TID (unit in volt)

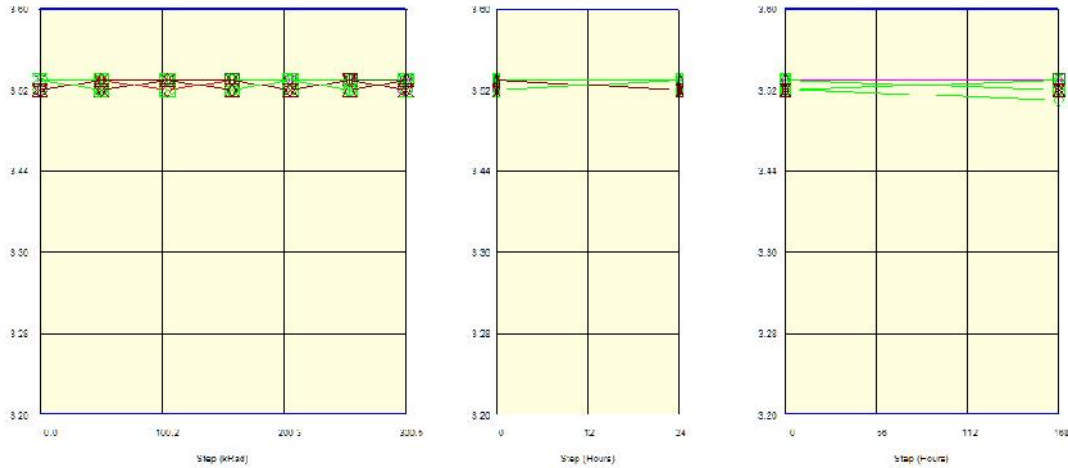


VIL BIDIR versus TID (unit in volt)

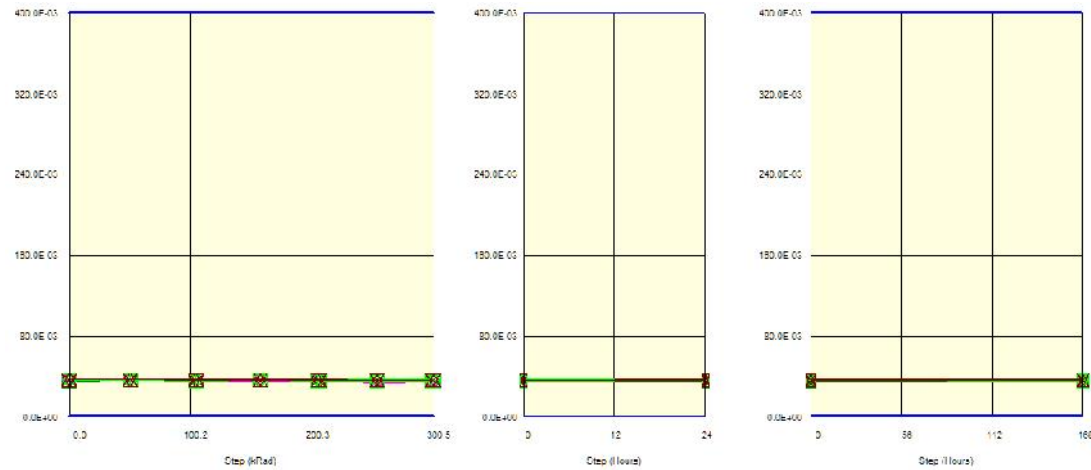


Schmitt trigger hysteresis versus TID (unit in volt)

IOs Characterization Results (I2C)



VOH versus TID (unit in volt)

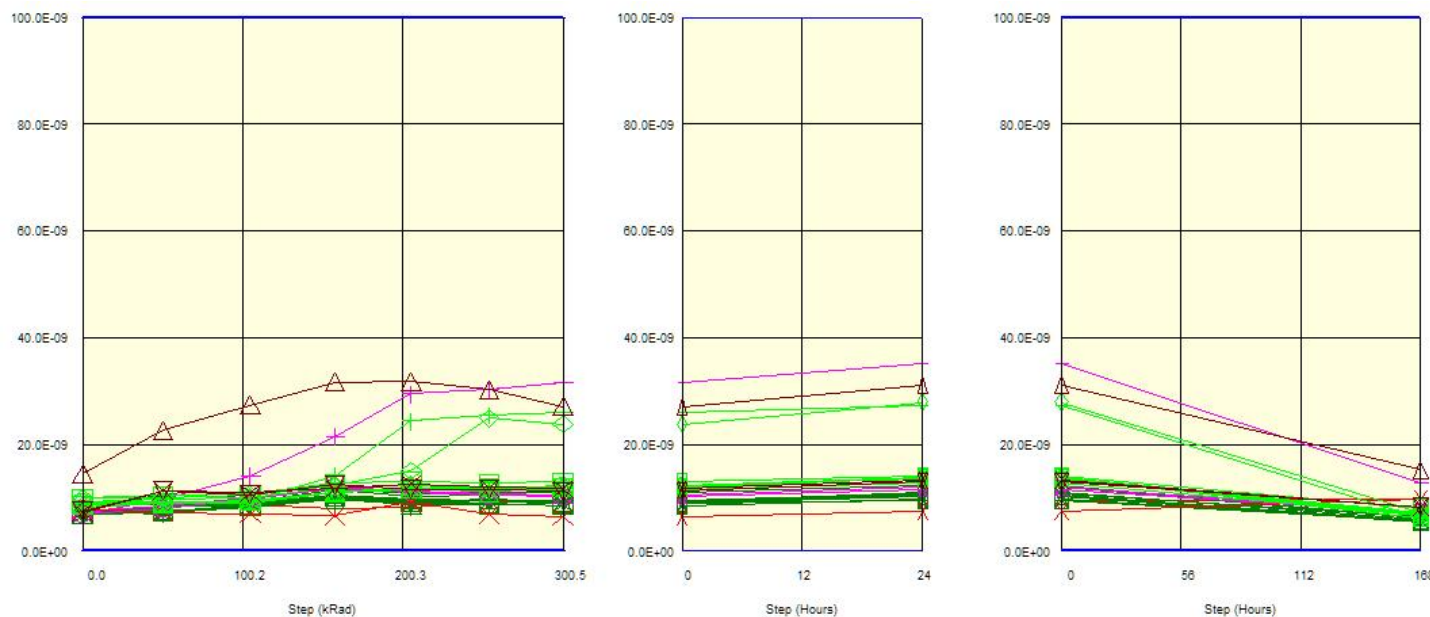


VOL versus TID (unit in volt)

Cold Sparing Characterization Results

Cold Sparing definition:

- Cold Sparing for space application has been defined in the case of devices redundancy, the backup devices don't influence the working device and so the device should present high impedance in respect of the active signal in order to avoid any distortion
- Based on several ESA studies and recommendations a device that embeds a cold sparing capability should present a minimum of 1M ohms impedance on its IO. Therefore the method consists in measuring and observing the leakage current while the device is not power up on different Ios, sourcing on these pins a nominal voltage of 1.2V.



Cold Spare versus TID (unit in A)

TID testing conclusions

- The two diffusion lots under TID testing behave the same. They are homogenous which confirms there is no process dispersion.
- No functional failure observed during the test and after annealing.
- IOs (LVDS, BIDIR and I2C):
 - No drift out of specification was observed up to 300 krad (Si).
 - Cold Sparing far below 100 nA max specification. Cold spare LVDS IO operates at 2.5V up to 650 Mbps.
- Lock time measurements:
 - An increase lower than 1% was observed on this parameter.
 - The worst case “Lock time” drift was observed on one biased sample with a time lock decrease of maximum 4%, i.e. from 38.1μs to 36.9μs after 300 krad (Si).
- Total Jitter measurements:
 - No drift out of specification was observed up to 300 krad (Si).
 - An increase of maximum 2% was observed on this parameter.
 - The worst case drift was observed on biased samples with a total jitter increase of 8% from 306ps to 322ps.
- Overall the PLL1201 is fully immune to TID at the maximum cumulated dose, here set to 300 krad (Si).

Reference: A 65nm STM Space-Grade ASIC Technology for Space Applications”, by L.Hili (ESA), P.Roche (ST), ESSCON, Noordwijk-ann-Zee, March 2016.

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Thank You !

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