ASSESSING RADIATION HARDNESS OF SIC MOS STRUCTURES

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→ MOTIVATION AND STUDY STRATEGY

This study aims to support the development of discrete European radiation hardened SiC power MOSFET for use in space applications by means of studying the gate oxide in terms of SEE and TID as one of the key parameters in the future development of these devices. The resistance of the P/N junctions present in these devices was also studied as well taking into account the problems seen in Schottky junctions under heavy ions radiation combined with high voltage.

The following approach to better understand SiC Power MOSFET sensitivity was followed:

- Gate Oxide oxidation process and gate geometry study: 3 oxidation processes + 5 gate geometries tested under gamma and heavy ions
- Heavy Ions test of 600V HV L-DMOS with experimental boron-doped gate oxide that could improve radiation hardness
- Heavy ions onto 1200V PIN diodes fully representative of the built-in ones present in power MOSFETs

→GATE OXIDATION PROCESSES & GEOMETRIES

DUTs description: SiC Lateral MOS

- Ox1: Thermally grown gate thin SiO2 oxide in N2O ambient + TEOS deposition 400 Å
- Ox2: Thermally grown gate SiO2 oxide + Boron doped 1 + TEOS 400 Å
- Ox3: Thermally grown gate thin SiO2 oxide in N2O ambient + TEOS deposition 400 Å with oxidation process optimization

DUT	Gate Width (µm)	Gate Length (µm)	Channel Rotation Vs flat (11-20) (°)
MOS1	2	150	0
MOS2	4	150	0
MOS3	24	150	0
MOS4	4	300	0
MOS5	24	150	30

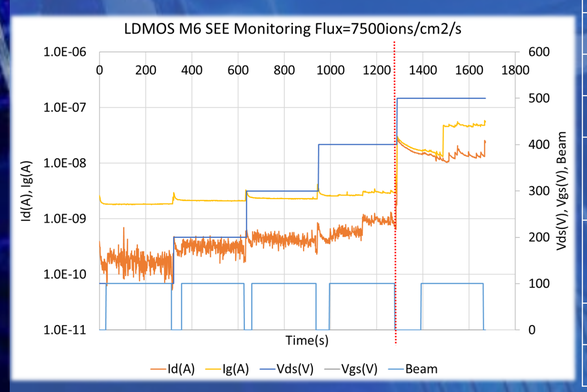
Results:

- No failures under heavy ions beams up to LET=62.5MeV /mg/cm^2
- Total recovery after annealing for gamma (300Krad)
- Small differences among oxide types and no difference among gate geometries

→ HV L-DMOS UNDER HEAVY IONS

Catastrophic damage of the devices for bias values as low as VDS=200V for LET values of 32.4 and VDS=400V for 20.4 MeV/cm^2/mg(Si). The damage occurs during radiation while biasing or during intermediate PIGS after a step.

Results:

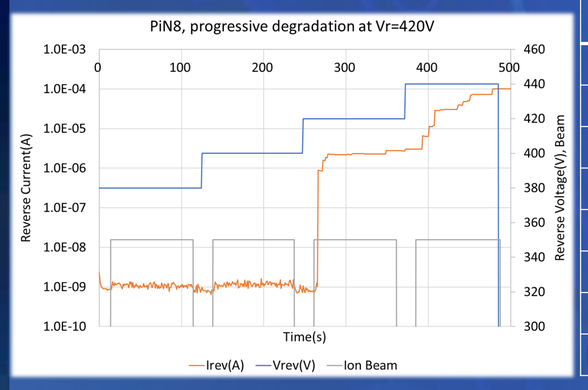


LET	V_{GS} (V)	V_{DS} (V)	Damage
10.0	0, 2.5, -5	0	no
20.4	0, 2.5, -5	0	no
32.4	0, 2.5, -5	0	no
10.0	0	up to 500	no
20.4	0	up to 500	PIGS after 400V run
32.4	0	up to 500	PIGS after 200V run
62.5	0	up to 500	200V run
20.4	-5	up to 500	400V run

→ PIN DIODES UNDER HEAVY IONS

Built-in diodes tested separately revealed the sensitivity of this area of the power MOSFET to heavy ions while HV is applied. Damage of the PIN occurs for reverse voltages slightly higher than for Schottky of previous studies.

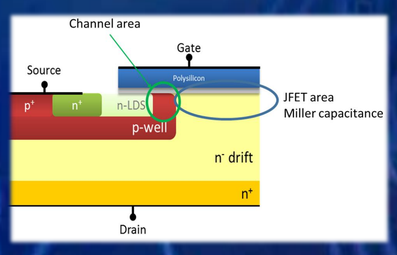
Results:



DUT	LET	Vrev Step (V)	Failure at
PiN1	10.0	100	abrupt failure @500V
PiN2	20.4	100	abrupt failure @500V
PiN3	32.4	100	degradation @400V
PiN4	62.5	100	degradation @400V
PiN7	20.4	25	degradation @400V
PiN8	20.4	20	degradation @420V
PiN9	32.4	25	degradation @400V
PiN11	32.4	20	degradation @400V

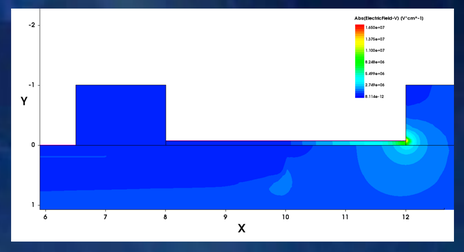
→CONCLUSIONS

- SEE testing of the lateral MOS revealed no sensitivity of the devices to heavy ions. A possible explanation for this could be that damage in vertical DMOS is mainly located in the JFET area between p-wells which is submitted to higher electric fields. No important differences could be detected comparing oxidation processes and gate geometries. However, slightly better behaviour under gamma radiation was observed for the devices with boron doped devices.

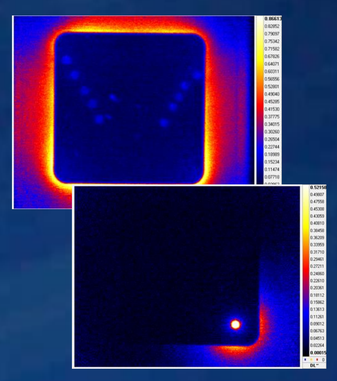


- SEE testing of the L-DMOS: In vertical power devices, the weak area is the JFET zone located below the gate between the p-wells. In the LDMOS, there is no JFET area as the top cell is not symmetrical. In these structures, the high peak of electric field is usually at the end of the gate metallization where probably was located the breakdown point during our campaign. While in vertical power MOSFETs, the breakdown is taking place in the bulk, either in the P-well junction or in the termination junction.

Modelling of the electric field distribution in the LDMOS at 500V clearly shows the peak electric field located at the end of the gate metal. A clear improvement of this device could be then to increase the oxide below the metal in the gate end. For the L-DMOS under test, the damage is located in a different area than in the vertical DMOS. This explains degradation happening during irradiation steps, while in a vertical structure, the damage is usually revealed during PIGS.



- SEE testing of 1200V PIN diodes revealed sensitivity to ions but better behavior than 1200 Schottky diodes. The dependence of the damage with LET is also lower for PIN diodes. Thermographic analysis of damaged devices shows different failure modes for different devices, observing both uniform damage in the junction area and local hot spots probably located in already defective spots of the crystal depending on the sample analyzed.



→ACKNOWLEDGMENTS

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