

Industrialisation and procurement of the ITER Interlock Discharge Loop Interface Boxes (DLIB)

Call for Nomination

Purpose

The objective of this contract is to complete the final design of the Central Interlock System (CIS) Discharge Loop Interface Boxes (DLIB) and procure the 150 units required for the ITER hardwired interlocks.

Background

The Interlock Control System of ITER is based on three different technologies: industrial PLC for the implementation of the slow interlock functions, FPGA-based COTS for the fast functions and current loops for the hardwired protections. This contract focuses on the later.

The interlock current loops (also called discharge loops) are hardwired connections between the different equipment involved on the protection of the ITER superconducting coils and associated systems. This includes the quench detectors, fast discharge units, protective make switches and AC/DC converters. When an interlock event requiring a fast discharge of the superconducting coils (e.g. magnet quench) occurs, the information is transmitted from the sensors to the actuators by the interruption of 3 redundant discharge loops.

In order to increase reliability and tolerance to spurious triggers, the loop is implemented using a 2oo3 voting architecture, meaning that two contacts are required to be activated, among the three available, in order to activate the interlock action of the corresponding discharge loop. This way in case of a single signal trigger the system remains working and the coils powered.

In order to standardise the implementation, simplify the interface design and maximise the whole interlock chain dependability the ITER Control System Division will provide a common mechanical and electrical interface to all the 'users' of these hardwired loops: the Discharge Loop Interface Box or DLIB (see Figure 1).

The base of the communication between the hardwired loop and the different actors is the DLIB. This electronic component has the main task of maintaining the continuity of the three wires of the loop, while interfacing the users of the loop. Each DLIB reads the states of each sensor or controller, provided also via three wires, and propagate the state to the loop (regenerating the 2oo3 voting if necessary) opening it or keeping its previous state. Depending on the case, it is configured to send the controller/actuator an 'open loop' state if the loop has been opened. This way the controller is able to react based on the state of the loop.

Each DLIB is also connected to a PLC (an existing or independent module, still to be defined, placed in the server room) for monitoring and testing purposes (not to interact or operate the DLIB during operation).

Intensive R&D program and prototyping campaigns have been carried out by IO during the last five years for obtaining an optimal design. Some of the DLIBs built during the last years are already being used in the field protecting real systems.



Figure 1: DLIB prototype

Scope of work

The contract is divided in two (2) phases:

- Phase 1 (1 year): from the existing design of the prototype DLIB V.3, industrialisation, validation of the design and construction of some pre-series units to provide green light for series production. This includes:
 - Evaluation of existing design and improvement
 - Industrialisation and cost estimation
 - Diagnostics definition and integration with CIS
 - Dependability study and SIL assessment
 - Obsolescence and maintenance plan
 - Environmental tests
- Phase 2 (1 year): procurement of the 150 DLIB units required for the tokamak hardwired interlocks. These may be delivered in two different batches after 6 months and at the completion of the contract.

Timetable

The tentative timetable is as follows:

Call for Nomination	December 2014
Receipt of Nominations	Late January 2015
Issuance of Pre-qualification	February 2015
Notification of Pre- qualification results	February 2015
Issuance of this Call for Tender	March 2015
Tender Proposals Due Date	May 2015
Estimated Contract Award Date	June 2015
Estimated Contract Start Date	July 2015

Experience

The contractor and its personnel shall have adequate experience in design of highly dependable electronic and mechanical components. This includes but is not comprehensive:

- Design and fabrication of electronics integrated circuits in special applications such as aerospace, nuclear power plants, fusion devices, High Energy Physics)
- Mechanical and electrical testing according to recognised international standards
- Experience in environmental qualification of electronics, (including Radiation and EMC)
- Dependability analysis for ASICs
- FPGA and Profinet solutions.

Candidature

Participation is open to all legal persons participating either individually or in a grouping (consortium) which is established in an ITER Member State. A legal person cannot participate individually or as a consortium partner in more than one application or tender. A consortium may be a permanent, legally-established grouping or a grouping, which has been constituted informally for a specific tender procedure. All members of a consortium (i.e. the leader and all other members) are jointly and severally liable to the ITER Organization.

The consortium groupings shall be presented at the pre-qualification stage. The tenderer's composition cannot be modified without the approval of the ITER Organization after the pre-qualification.

Legal entities belonging to the same legal grouping are allowed to participate separately if they are able to demonstrate independent technical and financial capacities. Candidates (individual or consortium) must comply with the selection criteria. The IO reserves the right to disregard duplicated reference projects and may exclude such legal entities from the pre-qualification procedure.