Harald Schone, Ph.D.

Jet Propulsion Laboratory, California Institute of Technology

Small Satellites Demand Innovation in Reliability

The Challenge of too Little Information

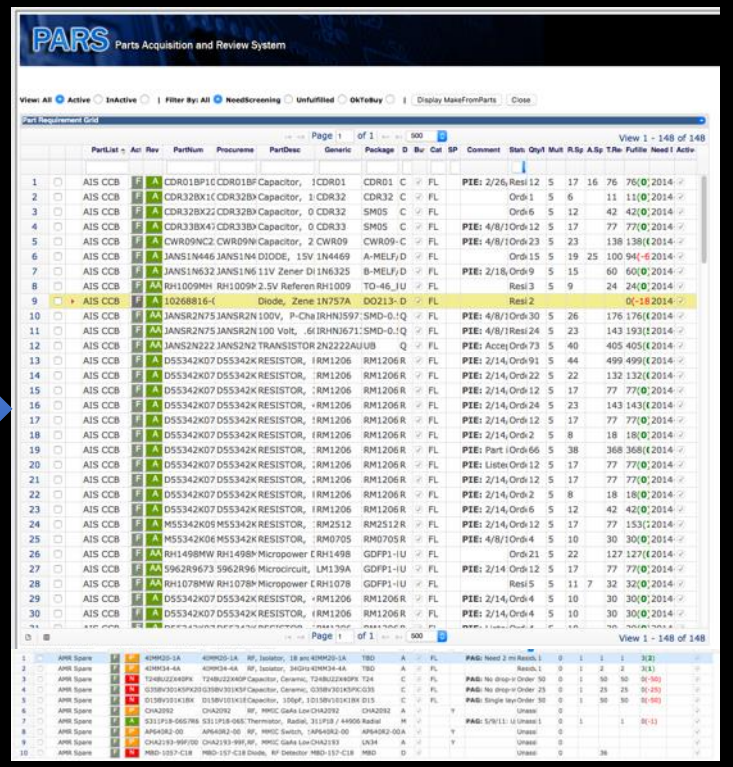
- Most COTS components are high quality
- Long term reliability for highly scaled CMOS is a concern
- Radiation data is typically unknown
- Design, process material, construction, etc. Information is useful, but vague
- Heritage rarely applies to COTS
  - No traditional lot traceability, frequent undisclosed design changes

Part Level Information Flow

ACCEDE COTS2019
SEVILLE – SPAIN 6-8 NOVEMBER

On a project the size of MSL:
~2000 unique electronic components

Test Data:
- Mil-Std 883
- Data Sheets
- Flight Heritage
- Radiation Tests
- Screening
- Burn-in
- Life test
- Stress tests
- …

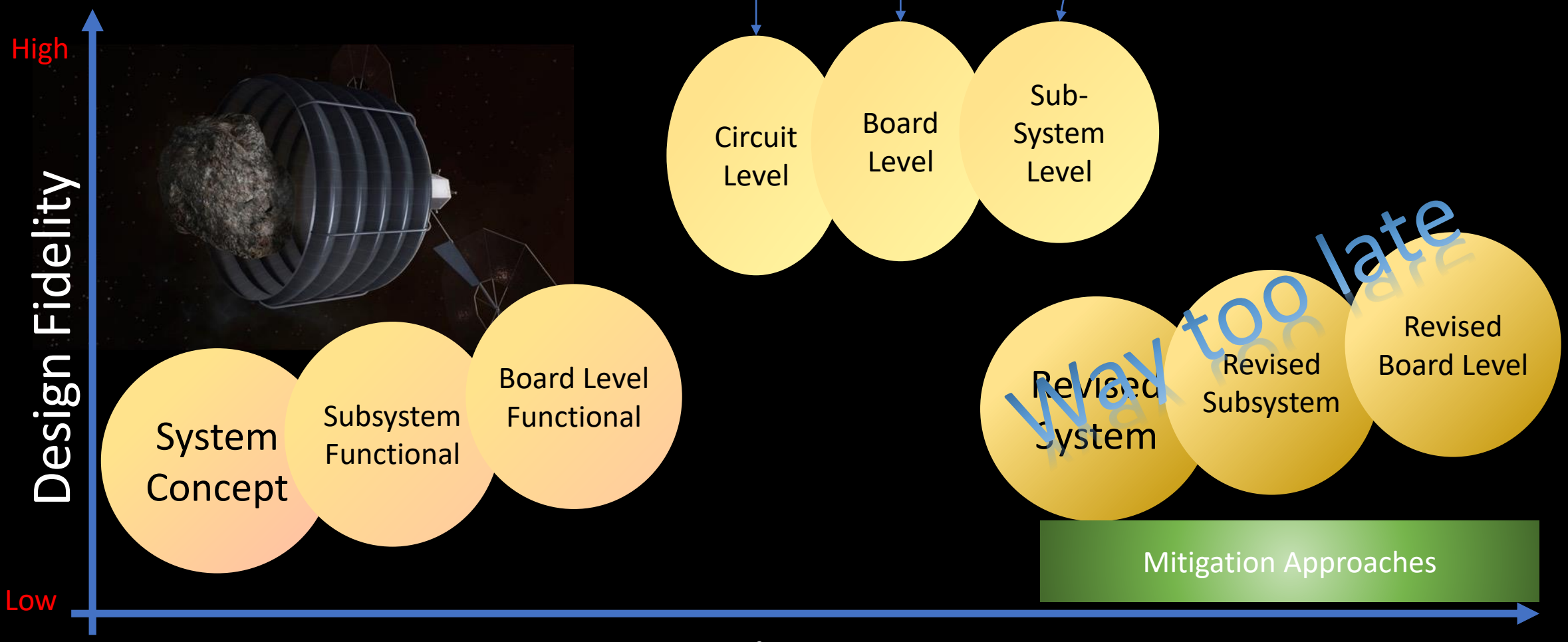


~100's components don't meet Mil-Std

Impact to project?
Likelihood?
Uncertainty?

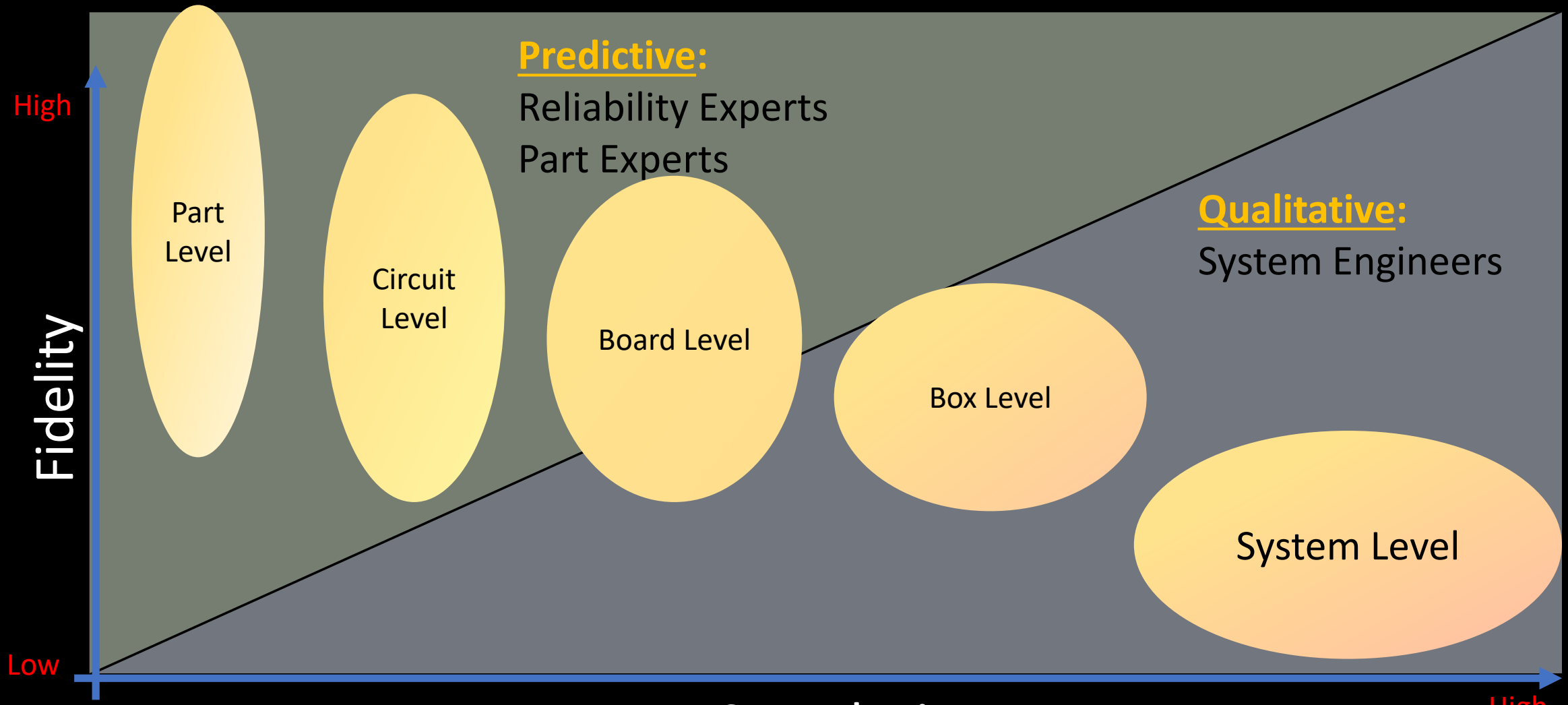
Mission Success is defined through high level capabilities-
Never by radiation effects!

Notional Design Flow vs. Reliabilty



Complexity vs. Model Fidelity

Crossing Expert Domains



Lowest Level of Fidelity: COTS Radiation Guideline

technology nodes). The primary design tradeoff for using these devices is that they are volatile, requiring an external configuration memory to store the configuration data; this adds design overhead, real-estate, power and additional reliability concerns to the system.

2.2.2 Flash-based architecture

A flash-based FPGA architecture replaces SRAM configuration elements with floating gate flash technology. The primary benefit being the configuration is non-volatile, meaning it is live on power-up and does not require external memory. The flash process is typically more efficient in terms of area and power. One drawback to flash-based FPGA is that the number of erase-program cycles is limited, unlike SRAM. However, that number is typically in the 10,000 to 100,000 range, which is more than enough for most space applications. Another drawback is that it is a non-standard CMOS process, meaning it will lag behind the aggressively scaled SRAM architecture. Microsemi, formerly Actel Corporation, is the main manufacturer of flash-based FPGAs.

2.2.3 Antifuse-based architecture

Finally, antifuse-based FPGAs implement one-time-programmable (OTP) switches to route and define logic elements. The advantages to this technology are its non-volatility and very small area overhead. The clear disadvantage is the inability to reprogram functionality, and the non-standard CMOS process required to produce the FPGAs. Microsemi and Aeroflex are the two primary manufacturers of antifuse FPGAs.

2.3 RADIATION EFFECTS ON FPGA TECHNOLOGIES

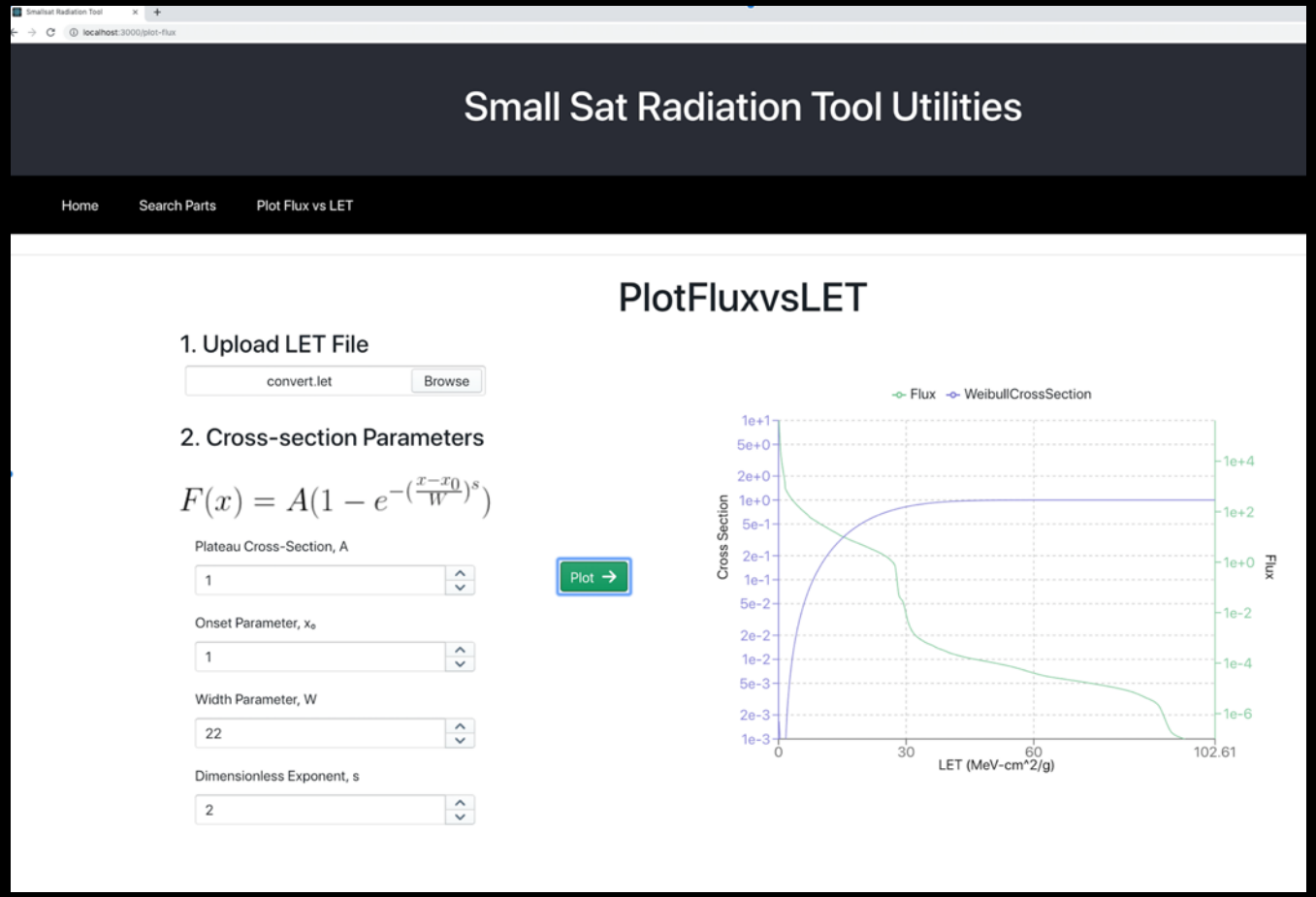
This section provides an overview of radiation effects on the three main FPGA technologies. While not intended to be a comprehensive review of radiation effects, the goal is to provide enough information to aid in the selection of the right COTS FPGA technology for a particular JPL flight mission and/or application.

2.3.1 Destructive Effects – Single Event Latchup – Any FPGA Containing CMOS

2.3.1.1 Overview

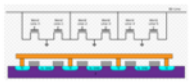
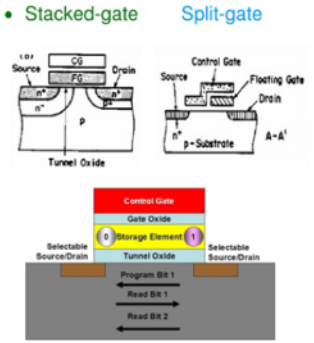
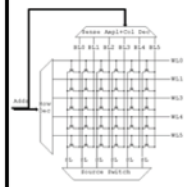
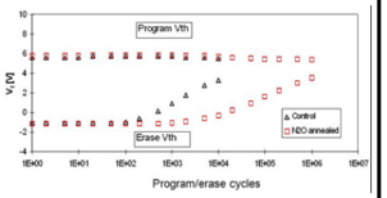
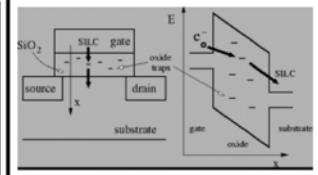
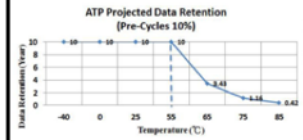
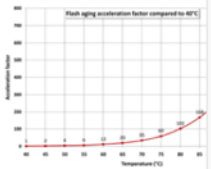
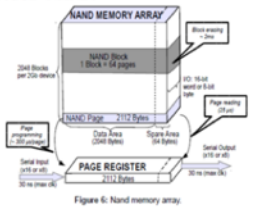
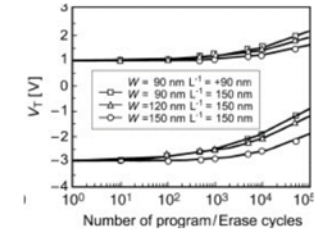
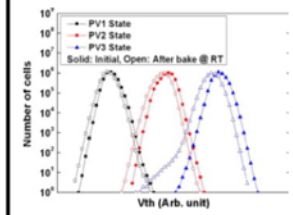
CMOS technology is potentially susceptible to single event latchup (SEL). SEL susceptibility in these devices can range from complete immunity, to very rare events, to extremely frequent and/or destructive events.

Rad Guidelines Codified in an Expert System



Lowest Level of Fidelity: COTS Reliability Guideline

M-2 Microcircuits

Type	*Overview/General Construction*	*Circuit Applications*	*Common Failure Modes*	*Failure Mechanisms*	*Technology Trends*	*Reliability*	*Recommendatio*
NVM, NOR Flash Single-level Cells 	split-gate-based. Floating-gate-based and split-gate-based use a floating poly-Si gate to store the data while the charge-trapping type uses nitride (Si_3N_4) for charge storage. They all employ channel hot electron mechanism to program and tunneling for erase. Generally available in TSOP and BGA packages. • Stacked-gate Split-gate 	its random access capability. Faster read and write compared to NAND Flash. Technology of choice for embedded applications. 	* Data retention due to charge loss at higher temperature (>150°C) * Over-erase bit causing excessive bit line leakage * Degradation of charge pump efficiency * Gate oxide rupture 	of trap sites and interface states inside oxide) from P/E cycling is the root cause of failures. * Stress induced leakage current (SILC) attributed to data retention failure 	data retention compared to both floating-gate and charge-trapping types. However, its density (~64Mb) is relatively small as compared to floating-gate and charge-trapping (~1Gb). The major Floating gate vendors are Micron, Atmal and Intel. Split gate vendor: Microchips (formally SST) Charge Trapping (Mirror bit) Vendor: Cypress (formally Spansion)	quality of the tunnel oxide. They are sensitive to P/E cycle, extended read conditions. 	PE cycles and operating temperature. easily degraded under excessive radia Recommend a derating factor of 0.75 rated endurance cycles from manufactu Use Hamming ECC at a minimum. Per cycling at min, max & nom. Vcc to fu over life for critical applications. 
NVM, NOR Flash Multi-level Cells	Only the Floating-gate and Charge-trapping type offer MLC (two bits per cell), e.g., Intel's StrataFlash and Spansion's mirror-bit technologies. Intel's StrataFlash employs different charge density in the floating gate to store 2 bits of information. Spansion's mirror bit employs charge trapped near the source and drain junctions to store 2 bits max. of information.	Widely used for code storage due to its random access capability. Faster read and write as compared to NAND Flash. Technology of choice for embedded applications.	* Read window closure due to excessive P/E cycle. * Data retention failure due to charge loss at higher temperature (>150°C) * Over-erase bit * Over-program bit * Gate oxide rupture	* Electron trapping and charging attributed to cycling-induced failures. * Stress induced leakage current (SILC) attributed to data retention failure.	Currently not widely offered by the vendors. MLC is typically offered for NAND-based Flash.	MLC NOR is generally less reliable than SLC. Typically the endurance spec will show a 10x difference (10K for MLC, 100K for SLC).	MLC Flash is not recommended for us application. Extra consideration need ECC.
NVM, NAND Flash Single-level Cells 	The basic storage cell in a mainstream NAND flash is similar to NOR. The key difference is how these storage cells are connected. For NAND, there are a total of 16 to 32 storage cells connected in series with two select transistors at the top and bottom of the string. NAND employs Fowler Nordheim tunneling mechanism for both program and erase. NAND SLC has a 2D planar topology compared to the more advanced 3D-NAND.  Figure 6: Nand memory array	Widely used for data storage, e.g., thumb drive, solid date disk drive) due to its low bit cost (< $1 per Gb).	* Read window is widening due to excessive P/E cycles. * Charge loss leading data retention failure at high temperatures. * Degradation of charge pump efficiency under radioactive environment. 	* Electron trapping and charging attributed to cycling-induced failures. * Stress induced leakage current (SILC) attributed to data retention failure. * High voltage operations resulting in severe cell-cell interference and program disturbs. 	2D NAND encounters scaling challenges at 10 to 19 nm node. Vendors have gradually migrated towards 3D-NAND topology to continue with the NAND scaling.	NAND shares common reliability problems with NOR. Cycling-induced oxide degradation is one major issue.	SLC NAND is considered to be more MLC NAND. The endurance spec for typically rated up to 10K cycles. Reco factor of 0.75 for Vmax, Imax and rate from the manufacturer's data sheet. A chip is typically introduced for giga-b (>Gb) for efficient and reliable data ma garbage collection, bad blocks). Use Reed-Solomon ECC. Perform end min, max & nom. Vcc to fully charact critical applications.
NVM, NAND Flash Multi-level Cells	Multi-level cells in 2D-NAND still adopt the SLC NAND string structure. The key difference is how the cells are programmed to different levels. Three types of multi-level cells are available - MLC (2 bits/cell), TLC (3 bits/cell) and QLC (4 bits/cell). For advanced 2D-NAND, the NAND string with 48-96 layers is	Widely used for data storage, e.g., thumb drive and solid state disk drive due to its low bit cost (< $1 per Gb).	* Read window widening due to excessive P/E cycles. * Charge loss leading to data retention failure at high temperate. * Degradation of charge pump efficiency under radiative environment.	* Electron trapping and charging attributed to cycling-induced failures. * Stress induced leakage current (SILC) attributed to data retention failure.	Transition of 2D-NAND towards 3D-NAND started in late 2016.	Reliability of MLC NAND is worse than its SLC counterpart. An obvious differentiator is the endurance specs: < 1K for MLC versus 10K for SLC.	MLC Flash is not recommended for us applications. Extra considerations ne

Appendix A | Capacitors | Diodes | Optoelectronics | Microcircuits | Resistors | Thermistors | Transistors | +

COTS Reliability Codified in Expert System

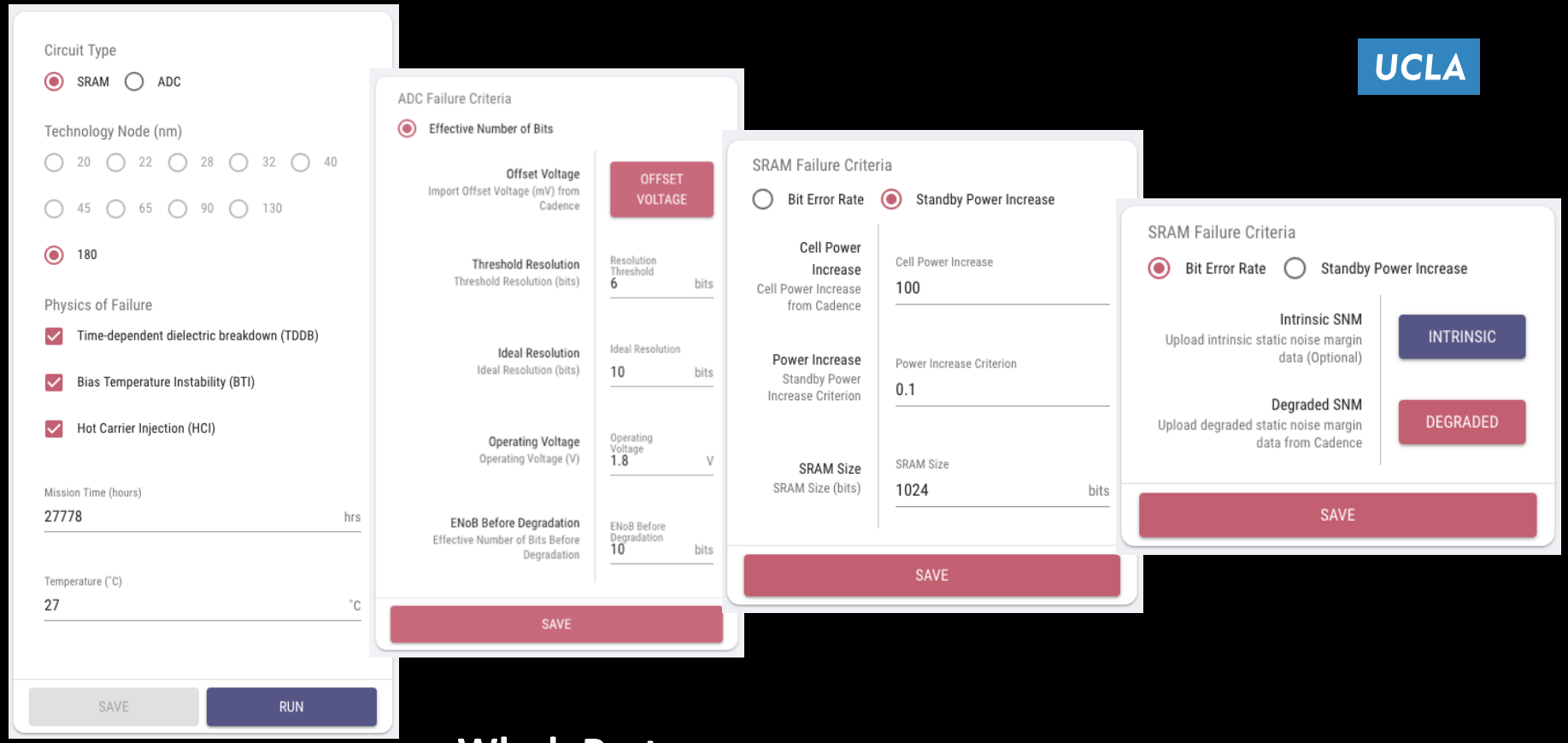
Automatically retrieves Intel Fab information to predict physics of failure

- Part Database
- Bayesian Estimation
- Circuit Simulation
- Process Factor

$(\lambda_{DB}, \lambda_{BE}, \lambda_{CS}, \alpha_{PF})$

ES performs:
Non-Homogenous and Linear α_{PF} adjustment

Prior: λ_{DB}
Likelihood: Results of BE (λ_{BE}) and CS (λ_{CS})
The final result will be adjusted by (α_{PF})

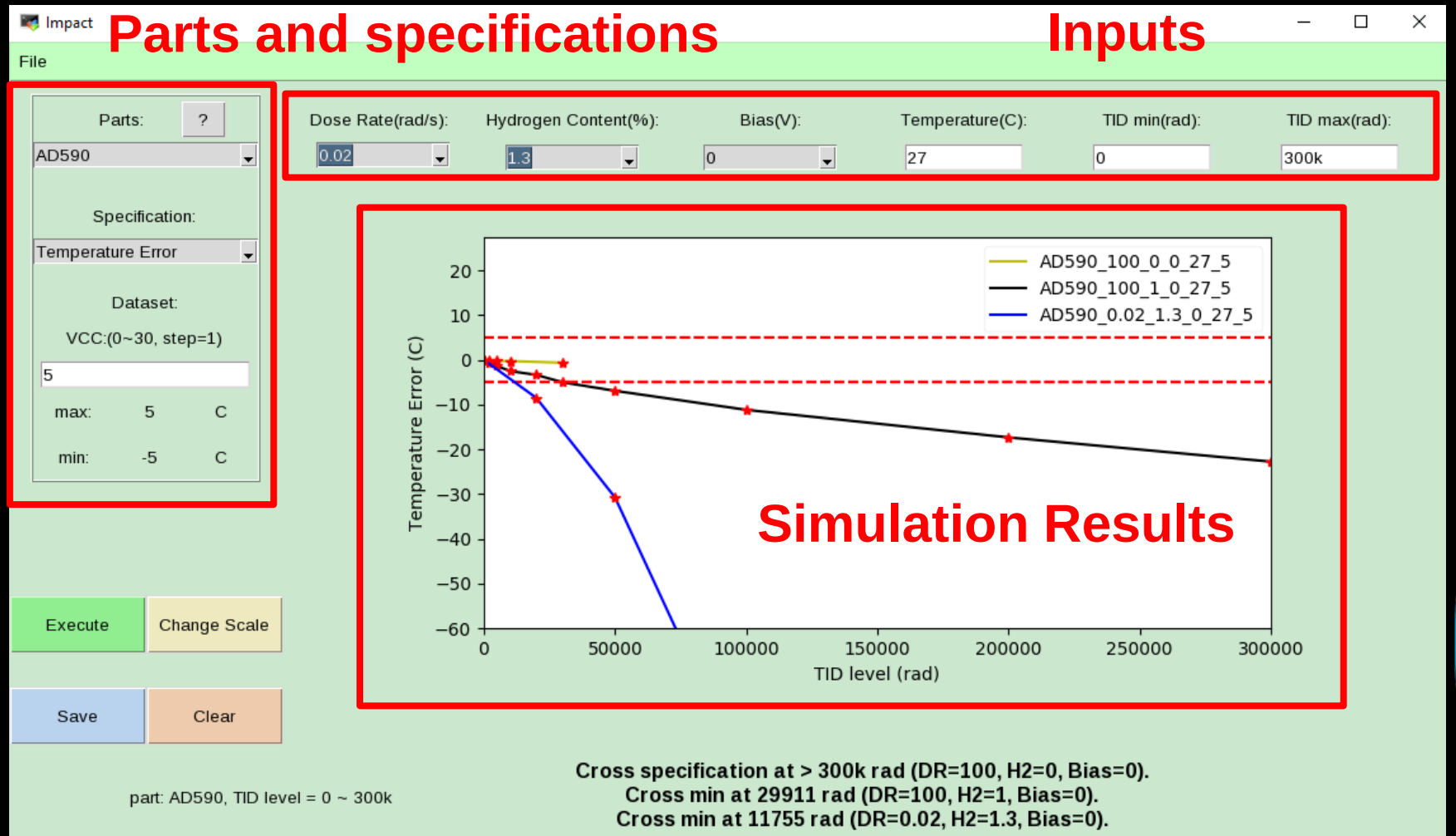


UCLA

WholeParts

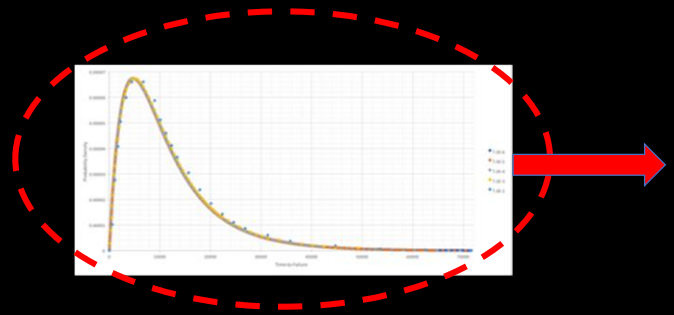
A JPL tool to troll the internet and automatically approve parts for flight
>500,000 parts already in database
>50% of JPL parts are automatically approved

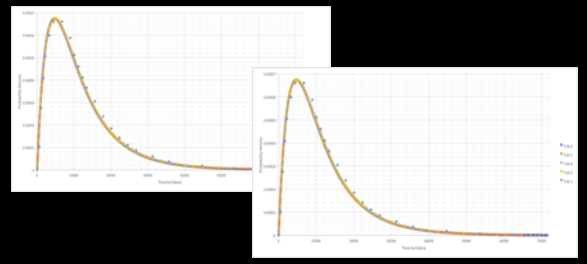
Predictive TID for Analog Devices: IMPACT



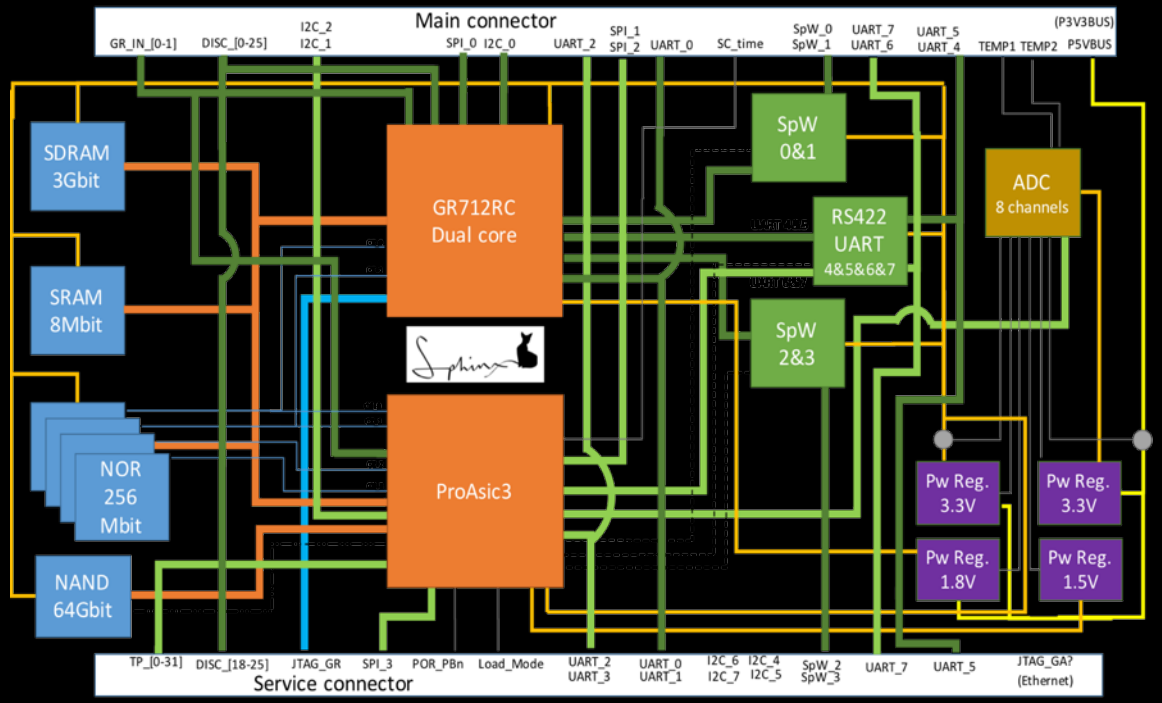
Libraries of ~100 analog circuits by 2020

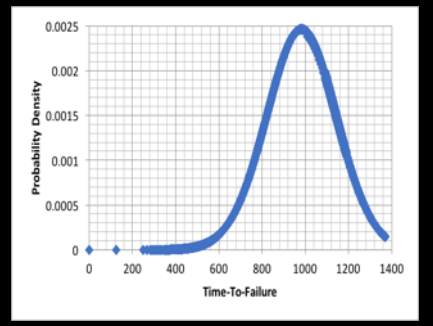
Predictive Rad Modeling at the circuit/board level





Component Reliability Metrics

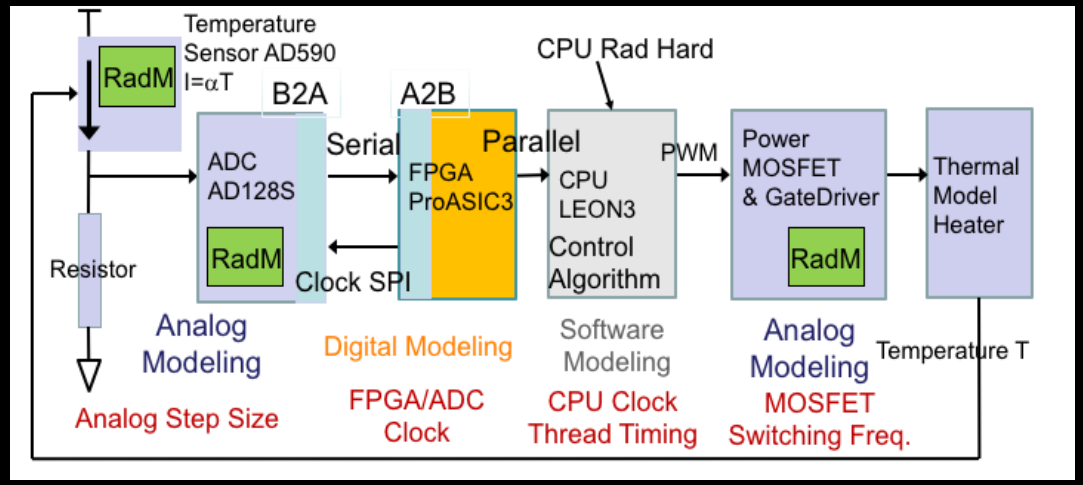




System Reliability Metrics

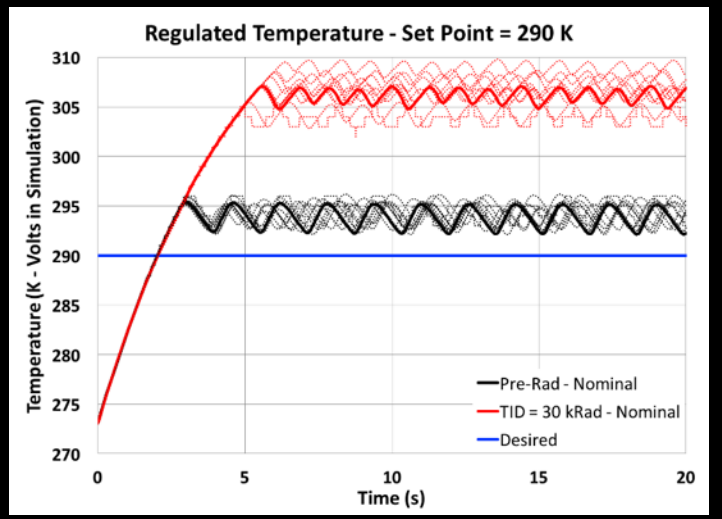
Predictive Rad Modeling at the circuit/board level

Temp. control loop within Sphynx C&DH



Rad modeling embedded in parameter variation

Closed-loop simulation results



Monte Carlo analysis included

System Level Model-based Assurance

Test data

Simulation Results

Standard Reliability

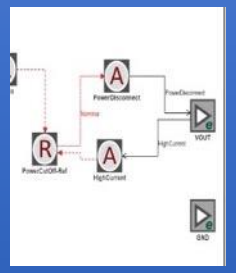
Selection Guidelines

Performance Specs

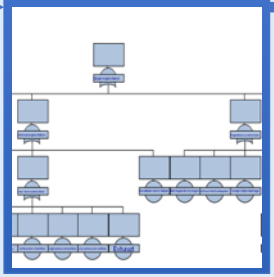
Compact Models

Requirements and Environments

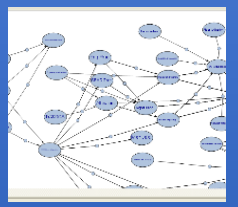
Functional description layer

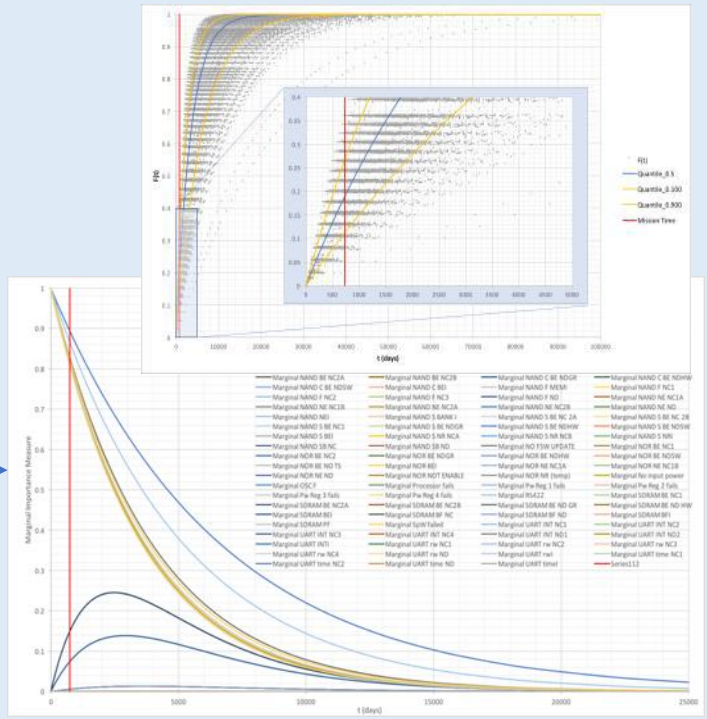


Fault propagation Layer



Quantitative layer





ASU

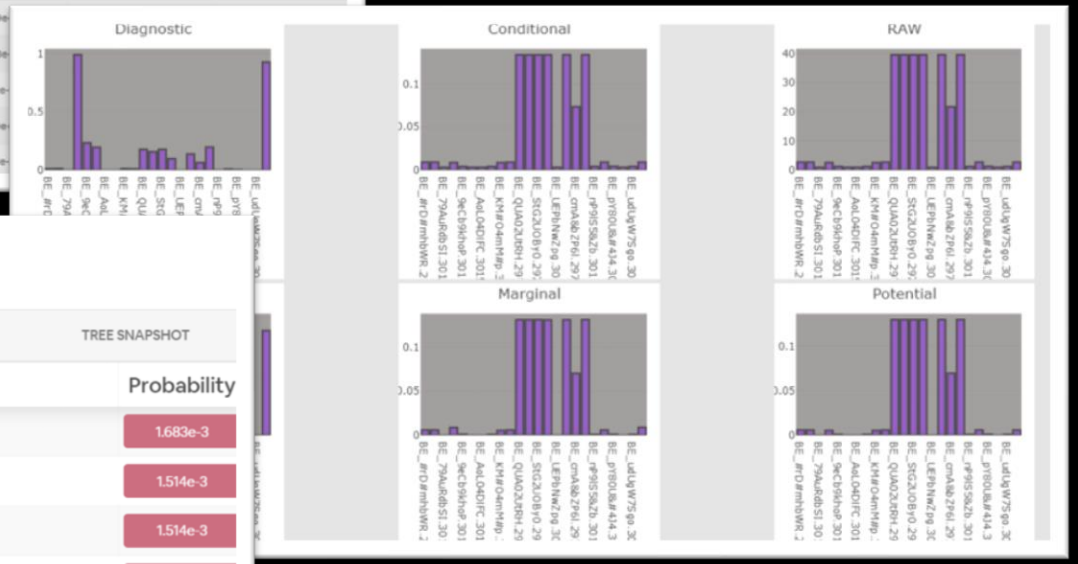
Jet Propulsion Laboratory
California Institute of Technology

Sandia National Laboratories

B. John Garrick Institute for the Risk Sciences
UCLA ENGINEERING

User Reports

Basic Event	Conditional	Marginal	Potential	Criticality	Diagnostic	RAW	RRW
Isolation Valve 22	1.498e-2	9.593e-3	9.550e-3	7.946e-3	1.241e-2	2.758e+0	1.008e+0
No 336.2 unavailable	1.498e-2	9.598e-3	9.550e-3	8.833e-3	1.379e-2	2.758e+0	1.009e+0
Secondary transformer	5.433e-3	6.024e-8	6.020e-8	6.262e-9	5.648e-4	1.000e+0	1.000e+0
LFD Delayed Response	0.000e+0	-8.762e-3	-5.433e-3	-6.129e-1	0.000e+0	0.000e+0	6.200e-1
Diesel Generator fails	6.929e-3	1.832e-3	1.496e-3	6.189e-2	2.341e-1	1.275e+0	1.066e+0
Operator fail to call	5.417e-3	-1.903e-5	-1.531e-5	-6.847e-4	1.949e		
Main transformer	5.434e-3	8.448e-7	8.448e-7	6.262e-9	4.028e		
Fuel levels low	6.929e-3	1.496e-3	1.496e-3	3.480e-10	1.612e-		
No response from LFD	0.000e+0	-5.460e-3	-5.433e-3	-5.025e-3	0.000e		
Pump 2 unavailable	1.498e-2	9.588e-3	9.550e-3	7.060e-3	1.103e-		



Quantified on Wednesday, 11 Sep 2019, 12:35

CUTSETS | IMPORTANCE MEASURES | CONFIGURATION | TREE SNAPSHOT

#	Minimal Cut Set	Probability
1	No. 336.1 unavailable, Operator fails to start pump 2	1.683e-3
2	Isolation valve 21 closed, Operator fails to start pump 2	1.514e-3
3	Isolation Valve 11 Closed, Operator fails to start pump 2	1.514e-3
4	Pump 1 Unavailable, Operator fails to start pump 2	1.346e-3
5	Detector/alarm actuator, Operator fails to start pump 2	1.178e-3
6	Tank Unavailable, Operator fails to start pump 2	8.414e-4
7	Offsite Power unavailable, Diesel generator fails to start	5.506e-4
8	No. 336.1 unavailable, No. 336.2 unavailable	2.500e-5
9	No. 336.1 unavailable, Isolation valve 22 closed	2.250e-5
10	Isolation Valve 11 Closed, No. 336.2 unavailable	2.250e-5

Conclusion

The (Unexpected) Benefits of Modeling

- Modeling can be a powerful RHA tool
- Make use of vague information
  - Expert knowledge can flow into model if properly weighted
- Effective way to collect information (standard format, metadata, C.C.)
- Enables information sharing
  - Sharing piles of papers, lists of lessons learned or best practices is cumbersome and discourages adoption
- A guide through a design/development/Ops process
  - Model fidelity needs to be adapted to stages in design