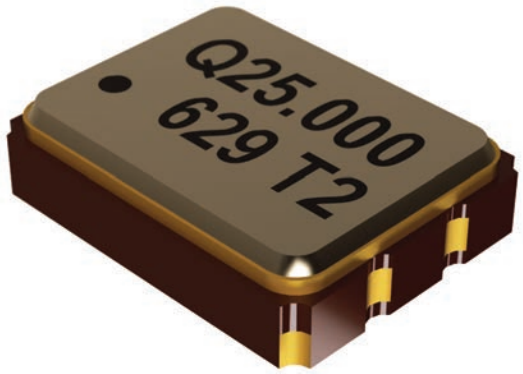
Description

Q-Tech's low profile extreme high shock hybrid oscillators consist of an IC operating at various supply voltages from 1.8V, 2.5V and 3.3V and a miniature strip quartz crystal. The series is offered in Surface-Mount SMT ceramic package. This is a small footprint package offered with a 50kRad(Si) TID for Low Earth Orbit (LEO) with high shock and high reliability space applications.



Features

- ECCN: EAR99
- 50kRad(Si) Total Dose Ionization
- Broad Frequency Range, 1.500MHz to 250MHz
- Small footprint, 2.5 x 3.2mm surface mount package
- CMOS Logic
- Various Supply Voltages, 1.8Vdc to 3.3Vdc
- Wide Operating Temperature Range, -55°C to 125°C
- Tri-State Output
- Hermetically sealed package
- Fundamental and 3rd Overtone Designs
- Screening per MIL-PRF-55310, Level B, with PIND
- High Shock Resistant, tested up to 20,000g Mechanical Shock, Half-Sine, 0.3ms, All Axes
- Tape and Reel Packaging is available for an additional cost
- Optional Hot Solder Dip, Sn60Pb40
- RoHS Compliant
- Screening and test data is not serialized.

Applications

- Commercial satellites
- Low Earth Orbit
- New Space

Ordering Information

(Sample part number)

Q T 735 L D 10 M - 50.000MHz

Q	T	723	L	D	10	M	-	50.000MHz

Solder Dip Options
T = Standard
S = Sn60Pb40

Package

Logic
L = CMOS +3.3V
N = CMOS +2.5V
R = CMOS +1.8V

Tristate
D = Tristate

Temperature code (*)
6 = ±50ppm at -55°C to +105°C
9 = ±50ppm at -55°C to +125°C
10 = ±100ppm at -55°C to +125°C
11 = ±50ppm at -40°C to +85°C
12 = ±100ppm at -40°C to +85°C
16 = ±100ppm at -55°C to +105°C
17 = ±100ppm at -40°C to +125°C
20 = ±50ppm at -40°C to +125°C

Screening
M = Screening per MIL-PRF-55310, Level B, modified
E = Engineering Model

Frequency
Output Frequency in MHz

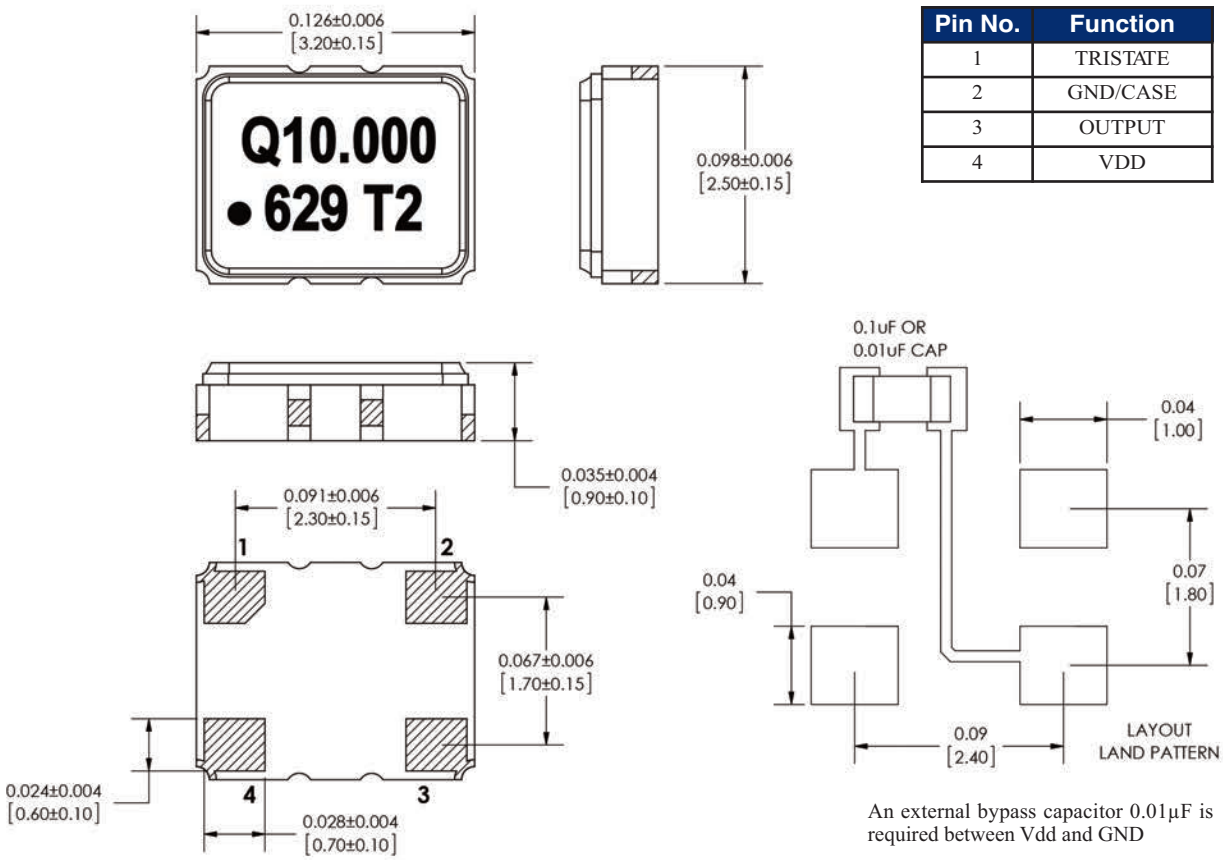
(*) Frequency stability vs. temperature codes may not be available in all frequencies.

Electrical Characteristics

Parameters	QT723L	QT723N	QT723R
Output frequency range (Fo)	**1.500MHz — 133.000MHz**	**1.500MHz — 125.000MHz**	
Supply voltage (Vdd)	3.3Vdc ± 10%	2.5Vdc ± 10%	1.8Vdc ± 10%
Maximum Applied Voltage (Vdd max.)	-0.5 to +5.0Vdc		-0.5 to +3.6Vdc
Frequency stability (ΔF/ΔT)	See Part Number on Page 1		
Operating temperature (Topr)	See Part Number on Page 1		
Storage temperature (Tsto)	-62ºC to +125ºC		
Operating supply current (No Load)	6 mA max. - < 20MHz 7 mA max. - 20MHz ~ < 40MHz 8 mA max. - 40MHz ~ < 50MHz 9 mA max. - 50MHz ~ < 80MHz 10 mA max. - 80MHz ~ < 100MHz 40 mA max. - 100MHz ~ 125MHz	4.5 mA max. - < 20MHz 5.5 mA max. - 20MHz ~ < 40MHz 7 mA max. - 40MHz ~ < 80MHz 7.5 mA max. - 80MHz ~ < 100MHz 30 mA max. - 100MHz ~ < 125MHz	2.5 mA max. - < 40MHz 3.5 mA max. - 40MHz ~ < 50MHz 6.5 mA max. - 50MHz ~ < 80MHz 7 mA max. - 80MHz ~ < 100MHz 20 mA max. - 100MHz ~ < 125MHz
Symmetry (50% of ouput waveform)	45/55%		
Rise and Fall times	4ns		5ns
Output Load	15pF max.		
Start-up time (Tstup)	5ms max.		
Output voltage (V_{OH}/V_{OL})	0.9Vdd min. / 0.1Vdd max.		
Output Current (I_{OH}/I_{OL})	± 4mA max. - <100MHz ± 8mA max. - ≥100MHz		± 2.8mA max. - <40MHz ± 4mA max. - ≥40MHz
Enable/Disable function Pin 1	VIH ≥ 0.7×Vdd (Active)		
	VIL ≤ 0.3×Vdd (High Z)		
Aging	±5ppm max. First Year ±2ppm max. Each Year Thereafter		

Package Outline and Pin Connections

Dimensions are in inches (mm)



Pin No.	Function
1	TRISTATE
2	GND/CASE
3	OUTPUT
4	VDD

An external bypass capacitor 0.01µF is required between Vdd and GND

Marking

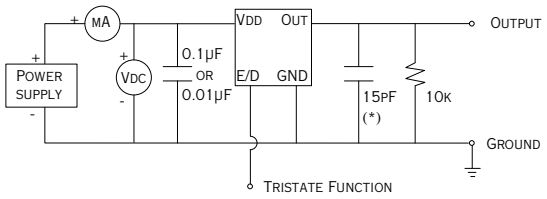
Line 1: QXX.XXX (Q for Q-Tech, no space 7 Characters of Frequency including decimal)
Line 2: Dot (Pin 1 Indicator) + Date code (Y/WW), Internal Traceability Code

Package Information

- Termination pads (4x), Electro nickel plating 1.27µm ~ 8.89µm typ., with gold 0.3µm ~ 1.0µm flash plate
- Weight: 0.025g typ.

Test Circuit

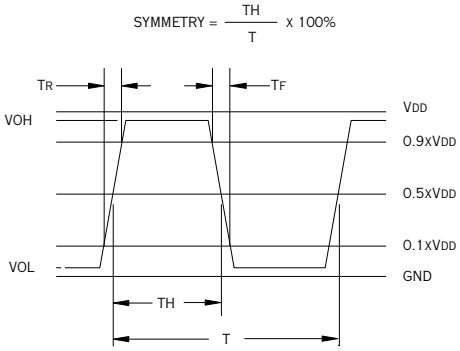
TYPICAL TEST CIRCUIT FOR CMOS LOGIC



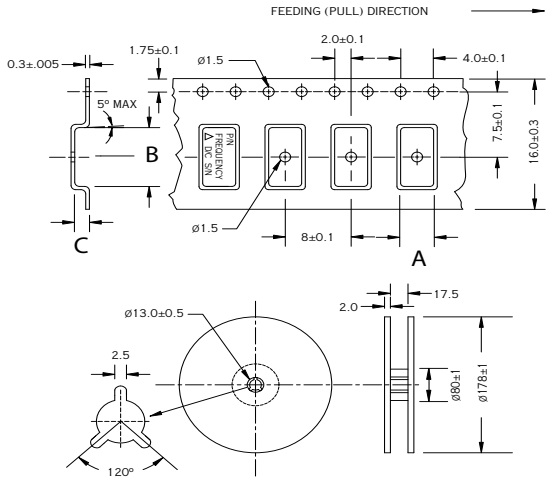
(*) CL INCLUDES PROBE AND JIG CAPACITANCE

The Tristate function on pin 1 has a built-in pull-up resistor so it can be left floating or tied to Vdd without deteriorating the electrical performance.

Output Waveform (Typical)



Embossed Tape and Reel Information



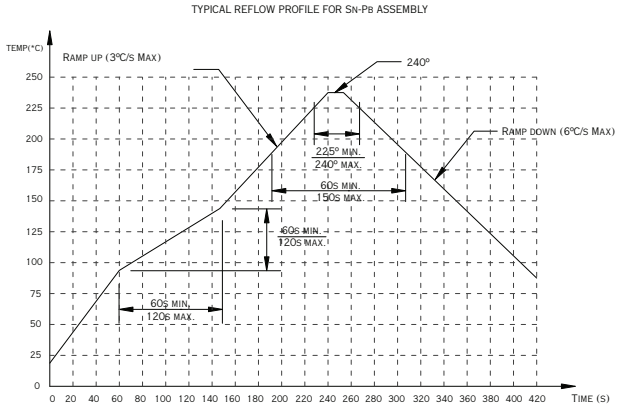
Dimensions are in mm. Tape is compliant to EIA-481-A.

Package	A	B	C
QT723	2.80 ±0.1	3.50 ±0.1	1.50 ±0.1

Reel size (Diameter in mm)	Qty per reel (pcs)
178	1,000

Reflow Profile

TYPICAL REFLOW PROFILE FOR Sn-Pb ASSEMBLY



SCREENING PER MIL-PRF-55310, LEVEL B PLUS PIND TEST

TEST	SPECIFICATION
Internal Visual	MIL-STD-883, Method 2017 and 2032
Stabilization Bake	MIL-STD-883, Method 1008, Condition C
Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Constant Acceleration	MIL-STD-883, Method 2001, Test Condition A, Y1 axis only
Particle Impact Noise Detection	MIL-STD-883, Method 2020, Test Condition B
Fine Leak	MIL-STD-883, Method 1014, Condition A1 (See Note 1)
Gross Leak	MIL-STD-883, Method 1014, Condition C
Pre Burn-In	Electrical Test (Optional)
Burn-In (load)	Nominal Supply, +125°C for 160 hours minimum
Final Electrical Test	Electrical test at +25°C and over temperature
External Visual	MIL-STD-883, Method 2009

NOTES:

1. Condition A1 Fine Leak Rate is $5x10^{-8}$ atm-cm^3/s Helium gas.

QUALITY CONFORMANCE INSPECTION TESTS (OPTIONAL)

GROUP	TEST METHOD	DESCRIPTION
A	MIL-PRF-55310, Level B, 100%	Electrical Tests (Supply voltage, Input Current, Output waveform, Rise and Fall times, Duty cycle, start-up time, overvoltage survivability, and 10 temperature frequency data points)
B	MIL-PRF-55310, Level B, 100%	Aging Test (Oscillator is energized in oven for a continuous period of 30 days at +70°C ± 3°C. The output frequency is measured within an interval of 72 hours maximum per MIL-PRF-55310)
C (Subgroups 1 to 4, excluding the "when specified" tests)	MIL-PRF-55310, Level B, sampling	4 (0)

ADDITIONAL INFORMATION

1) Design used a Class B integrated circuit, with Radiation features 50kRad(Si) Total Ionizing Dose and a high Q cultured quartz.
2) ESD HBM Class 1C.
3) Standard packaging in anti-static plastic tube.
4) Screening and QCI data shall not be serialized.

DCO	REV	REVISION SUMMARY	PAGE	DATE
10413	-	Initial Release		09/11/2019