3rd BRAVE FPGA DAYS

NX workshop - 26-27nov19
+ 1:1 meeting - 28nov19
ESA/ESTEC Noordwijk, NL

NanoXplore offers competitive European rad-hard FPGAs enabling systems flexibility, high performance and miniaturization.

Following the last 2 successful 'BRAVE FPGA Day' workshop in ESA/ESTEC Noordwijk, NL, the 3rd BRAVE Day is coming.

1st BRAVE FPGA Day done in Sep-2017 was an introduction to NanoXplore FPGA solutions.
2nd BRAVE FPGA Day done in Nov-2018 focused on 1st experiences and incoming Flight Heritage.

The 3rd BRAVE FPGA Day will introduce

- NX product marketing strategy, including our positioning on **NEW SPACE** market following the selection of NX within a Mega-Constellation of Satellites.
- NXmap roadmap including incoming NXmap-v3 major update
- NX product update on qualification, radiation performance including dedicated flow for New Space for:
  - NG-Medium
  - NG-Large
  - NG-Ultra
- New rad-hard FPGA device ULTRA-150.
- NX ecosystem update including
  - IP cores and Tools linked to NX products
  - End-users experience

NanoXplore

3rd BRAVE FPGA DAYs - 26nov19 - NX workshop Agenda

Time	Part 1 / NX news	Company	Who
08.30 – 09.30	Registration		
09.30 – 09.40	BRAVE Day introduction	ESA + CNES	David MERODIO + David DANGLA
09.40 – 10.10	NanoXplore Strategy	NX	Edouard LEPAPE
10.10 – 10.40	New Space Strategy: Why using COTS devices when Low-Cost RHBD FPGAs are available?	NX	Joël LE MAUFF
10.40 – 11.10	Product roadmap update	NX	Joël LE MAUFF
11.10 – 11.30	Break		
11.30 – 11.50	NXmap status	NX	Mohamed GOUNTAF
11.50 – 12.10	NXmap v3 overview	NX	Sylvain DEPIERRE
12.10 – 12.40	Demo: NXmap-v3, NXcore, NXscope	NX	Mohamed/Sylvain
12.40 – 13.00	NXmap Design Suite Q&A	NX	Mohamed/Sylvain
13.00 – 14.00	Lunch		

Time	Part 2 / Eco-System - IPcores	Company	Who
14.00 – 14.30	Adentis IPs to interface a MIL-ST-1553 bus	ADENTIS	Philippe MERCIER
14.30 – 15.00	Radiation Intelligent Memory Controller DDR2	3D-PLUS	Charles SELLIER
15.00 – 15.30	IP core portfolio and activities on NX devices	IngeniARS	Daniele DAVALLE
15.30 – 16.00	Break		
16.00 – 16.30	GRLIB IP Library	COBHAM Gaisler	Jan ANDERSSON
16.30 – 17.00	SpaceWire & SpaceFiber	STAR Dundee	Steve PARKES
17.00 – 17.30	PicoSky-FT processor inside NXcore	Skylabs	Dejan GACNIK

Time	Demo Session	Company	Who
17.30 – 19.00	Demo Session / Exhibition	Exhibitors	3D-PLUS MATHWORKS DAITEQ
19.00	End of 1st day		

20.00 – BRAVE FPGA Day dinner at Noordwijk, NL.
(each attendee will support the dinner at own expenses.
⇨ Thanks to register latest Tuesday the 26th 12am).

3rd BRAVE FPGA DAYs - 27nov19 - NX workshop

Time	Part 3 / Eco-System - Tools	Company	Who
08.30 – 09.00	Registration		
09.00 – 09.30	Model-Based Design in Space, what can we learn from other industries?	Mathworks	Stephen VAN BEEK
09.30 – 10.00	Accurate Estimation of NXmap Circuit Performance and Reliability by Static Analysis	Politecnico di Torino	Luca STERPONE
10.00 – 10.30	Towards Supporting Time and Space Partitioning Architectures in BRAVE MPSoCs (Large and Ultra): The XtratuM Approach	FentISS	Paco GOMEZ MOLINERO
10.30 – 11.00	Break		
11.00 – 11.30	The SpaceStudio NG-Ultra virtual platform	SpaceCo Design	Guy BOIS

Time	Part 4 / User Experiences	Company	Who
11.30 – 12.00	Image Processing Board for Space Exploration Autonomous Navigation based on NX FPGAs	GMV	David GONZALES ARJONA
12.00 – 12.30	CoRA-MBAD: A model based Avionics design environment for HW/SW Co-Design	Politecnico di Milano	Fabrizio FERRANDI
12.30 – 13.00	NG-Medium Remote Configuration	ALTRAN	Vincent THIBAULT
13.00 – 14.00	Lunch		

Time	Part 5 / Products	Company	Who
14.00 – 14.30	High-Performance Strategic European Building Block	ADS	Marion LE PENVEN
14.30 – 15.00	First European Space Computer Core: FUSIO RT	3D-PLUS	Coralie DANG-FELLER
15.00 – 15.30	Europonder : European High-Throughput Transponders, with NX FPGAs inside	SpaceChips	Rajan BEDI
15.30 – 16.15	Users request for tomorrow Platforms & Payloads	NX	ALL
16.15 – 16.30	Wrap-up		
16.30	Close 3rd BRAVE FPGA Day		

3rd BRAVE FPGA DAYs – 28nov19 - 1:1 MEETING

Hopefully, the 3rd BRAVE FPGA Days will give you a good overview about NX RHBD FPGA devices developments on both HW and SW sides.
Nevertheless, if you want to address specific topic with us, feel free to register to our 1:1 face meeting the 28nov19.

If you are interested to meet us, please register for a 30mns or 1h time slots below and feel free to tell us in advance your main topics to cover.

- ⇨ Product planning?
- ⇨ NXmap v2 or v3 issues?
- ⇨ Project management?
- ⇨ Quality issues?
- ⇨ Pricing?
- ⇨ Etc.

TIME	COMPANY	Name - Title	Main Issues	Project
08.00 – 08.30	OPEN			
08.30 – 09.30	**BOOKED**			
09.30 -10.00	BOOKED			
10.00 – 11.00	BOOKED			
11.00 – 11.30	OPEN			
11.30 – 12.00	OPEN			
12.00 – 13.00	OPEN			
Lunch				
14.00 – 14.30	OPEN			
14.30 – 15.00	OPEN			
15.00 – 15.30	OPEN			
15.30 – 16.30	**OPEN**			
16.30 -17.00	OPEN			
17.00 – 17.30	OPEN			
17.30 – 18.00	OPEN			

Please register to joel.lemauff@nanoxplore.com.

Please register to the event, by sending an email to the NanoXplore contact joel.lemauff@nanoxplore.com including ESA and CNES contacts in copy.

Participation to the event is free of charge but registration is required to get access to ESTEC.

Location: ESA/ ESTEC (Newton)
Date: 26-27 November 2018
Fee: Attendance to the workshop is free of charge
Organizers/ Contact persons:

NanoXplore: joel.lemauff@nanoxplore.com
ESA: david.merodio.codinachs@esa.int
CNES: david.dangla@cnes.fr

As last year, in parallel to the workshop, a maximum of 6 NanoXplore partners will exhibit. Please feel free to send an email to joel.lemauff@nanoxplore.com if interested.

And don't forget to also take the opportunity to attend the GR740 user day right after the BRAVE Day!

ABSTRACTS PART-2 / Eco-System – IP cores

- ## 2A- Adentis IPs to interface a MIL-ST-1553 bus

  Company: ADENTIS (FR)
  Speaker: Philippe MERCIER

The Mil-std-1553 bus is widely used in space and aeronautic applications. Adentis is proposing 2 IPs that facilitates the implementation of an interface to the Mil-std-1553 bus into an FPGA :

- The Mya-53RM2-IP implements a remote terminal interface,
- The Mya-53BRM2-IP implements a bus controller/remote terminal interface.

These 2 IPs have a long heritage in space domain and are now available in the Brave technology.

- ## 2B- Radiation Intelligent Memory Controller DDR2

  Company: 3D-PLUS (FR)
  Speaker: Charles SELLIER

RIMC DDR2 stands for Radiation Memory Controller DDR2.
This IP Core is much more than a simple DDR2 controller, it also protect the DDR2 from radiation effects such as SEU and SEFI.

User interfaces:

- AMBA (AHB and/or AXI for memory access, APB for the IP Core configuration)
- Bypass Interface

Some Key benefits from this IP Core:

- supports different types of ECC for data width applications from 8b up to 128b, providing SEU mitigation and SEFI protection.
- RIMC DDR2 Single Event Upset (SEU) mitigation uses different configurable ECCs (Hamming or Reed-Solomon) and scrubbing to correct SEUs and Single Event Row Errors (SERE).
- Verification tests have been performed to confirm the robustness of this protection IP, and no SEFI were observed up to LET>60Mev-cm^2/mg.
- Padding for memory initialisation
- Scrubbing mechanism embedded to avoid SEU/MBU accumulation
- Frequency configuration

- ## 2C- IP cores for Satellite High-Speed On-Board communication and telecommunications: IngeniARS IP core portfolio and activities on NX devices

  Company: IngeniArs S.r.l. (IT)
  Speaker: Daniele DAVALLE

IngeniArs S.r.l. is an Italian SME company established in 2014 as a spin-off of the University of Pisa and is based in Pisa. The main expertise of the company is the design of digital IP cores for FPGAs/ICs and relative test equipment.
IngeniArs has reached a number of important achievements that allowed the development of its IP core portfolio. To mention the most relevant: the successful Horizon 2020 SME

instrument project named “SIMPLE” has accelerated the development of SpaceFibre IP core and related test equipment; “IP core for medium data-rate PDT” ESA project allowed to develop the CCSDS 131.2-B-1 encoder and modulator IP core.
This presentation will be focused on the main IP cores of the IngeniArs portfolio, including:

- **CCSDS 131.2-B-1 encoder and modulator** for scientific telemetry downlink, featuring SCCC encoding and modulations such as (Q/8)PSK and (16/32/64)APSK.
- **SpaceFibre CODEC and router**, to enable high-speed serial communications among spacecraft subsystems.
- **WizardLink**, IP core equivalent to TI TLK2711 chip at interface level, is capable of replacing TI chip by using a SERDES available on the target FPGA.
- **SpaceWire CODEC and router**, the standard solution for on-board communications up to 200 Mb/s.

As part of the CCSDS 131.2-B-1 encoder modulator IP-core technology mapping, the IP core was characterized on NanoXplore devices, and the results of this activity will be presented as well.

- ## 2D- GRLIB IP Library

  Company: COBHAM Gaisler (SW)
  Speaker: Jan ANDERSSON

Cobham Gaisler provides the GRLIB IP library that includes the LEON3FT and LEON4FT processors, memory controllers, communication controllers and other peripheral IP. The presentation will cover the latest IP additions to the library and detail the extensions made to the GRLIB IP Library to allow users to rapidly target designs to NX FPGAs.

- ## 2E- SpaceWire and SpaceFibre

  Company: STAR-Dundee Ltd (UK)
  Speaker: Steve PARKES

STAR-Dundee has been working with NanoXplore on the implementation of SpaceFibre in the NG-Large FPGA. This work included early simulation of the SerDes model with SpaceFibre to ensure that the NG-Large FPGA would be fully compatible with SpaceFibre. It is expected that the first tests in NG-Large silicon can be presented. The broader range of STAR-Dundee SpaceWire and SpaceFibre IP cores and related SpaceWire and SpaceFibre test equipment suitable for use with NanoXplore FPGAs will be presented. This will include the very latest SpaceFibre test equipment from STAR-Dundee which is able to handle SpaceFibre traffic at very high data rates.

- ## 2F- PicoSky-FT Processor IP inside NXcore

  Company: SKYLABS (Si)
  Speaker: Dejan GACNIK

The only European small-foot print PicoSky-FT processor IP core has been successfully utilized in various SoC implementation in NX-Medium FPGA technology. Radiation performance has been performed with high energy neutrons at ChipIR and results of NSEE testing will be presented. The flexibility of the PicoSkyFT IP core and variety of complementary peripherals units, co-processors, hardware accelerators, communication interfaces, etc. make PicoSkyFT technology highly interesting for the Space industry and many others. Thus, the PicoSkyFT is becoming an importnant part of NXcore library, which furthermore exploits the benefits of both NG-Medium and PicoSkyFT processor

ABSTRACTS PART-3 / Eco-System – Tools

- ## 3A- Model-based Design in Space, What can we learn from other industries?

  Company: Mathworks (NL)
  Speaker: Stephen VAN BEEK

Speeding up the development process and 'zero defects' when targeting FPGAs and SoCs is mission critical in the (new) space industry.

Most companies in Automotive and Avionics industry have adopted simulation and verification techniques ensuring correctness of models and generated code. It abstracts complex behaviour for better understanding and with simulation verifies the design earlier on the desktop prior to hardware availability.

In this presentation we will discuss how these techniques can be applied on Space/FPGA applications to ensure 'zero defect' space missions.

- ## 3B- Accurate Estimation of NXmap Circuit Performance and Reliability by Static Analysis and Simulation

  Company: Politecnico Di Torino (IT)
  Speaker: Luca STERPONE

The Politecnico di Torino team is developing, in the framework of the EU Project VEGAS, a set of CAD tools to elaborate and analyse the netlist generated by the NXmap tool. In this presentation we will focus on the development of two tools: a static-analyzer of the post-layout netlist generated by NXmap and a Fault Simulator able to work on the NG-MEDIUM logic library. The two tools are effectively compatible with the last version of the NXmap software. The presentation will demonstrate the effective usage on the analysis of performance of the implemented circuit using the NXmap tool chain and we will demonstrate the possible application on the verification of robustness and mitigation techniques applied on a set of test-bench circuits implemented on the NG-MEDIUM device. Experimental results obtained by simulation will be commented and discussed in details.

- ## 3C- Towards Supporting Time and Space Partitioning architectures in BRAVE MPSoCs (NG-Large and NG-Ultra): The XtratuM Approach

  Company: FentISS (SP)
  Speaker: Paco GOMEZ MOLINARO

FENTISS has developed a new version of XtratuM, called XtratuM/NG (aka XNG) carefully optimized to run in ARM-Cortex processors. XNG is currently ECSS level B qualified over ARM-Cortex R5 and A9 and it has been selected by Airbus OneWeb Satellites as the basis for their Time and Space Partitioned On-Board Software Architecture.
This presentation proposes an approach to efficiently port XNG to the BRAVE Large and BRAVE Ultra MPSoC, identifies the main difficulties to mitigate processor interference when accessing shared resources, and outlines some techniques to achieve a high degree of optimization. Supporting RTEMS as guest-OS in XNG partitions is also described. Some

considerations on the space qualification (ECSS level B) of the resulting hypervisor are finally presented.

- **3D- The SpaceStudio NG-Ultra virtual platform**
  Company: Space Codesign Systems (CA)
  Speaker: Guy BOIS

The SpaceStudio technology is a development environment for designers that eases the design flow of advanced algorithms targeting FPGA technology while hiding the inherent complexity of FPGAs. In this talk, we present the SpaceStudio NG-Ultra virtual platform by focusing on HW/SW co-simulation and performance analysis. First results of experimentation will also be presented. Finally, we talk about next steps of development, mainly the integration of legacy functions (e.g., RTL code) in the co-simulation process and the support of third-party tools like High Level Synthesis (HLS) and Real Time Operating Systems (RTOS). This work is done within the context of the NAVISP project entitled Agnostic Hardware/Software codesign Framework for GNSS Software Receiver

ABSTRACTS PART-4 / User Experiences

- ## 4A- Image Processing Board for Space Exploration Autonomous Navigation based on NX FPGAs

  Company: GMV (SP)
  Speaker: David GONZALEZ ARJONA

We take the opportunity of showing an overview of the development of ***GMV's Image Processing Board (IPB) coprocessor hardware*** for Space Exploration related activities in the frame of an autonomous vision-based navigation system for satellite search & rendezvous operations and for Descent and Landing into small bodies. The IPB is based on GMV expertise and work in **CAMPHORVNAV, HERA** and **MSRDD** ESA's projects where developed IPB *offloads the GNC CPU load* and *accelerates the computer-vision algorithms* to reach the required operation frequencies for the autonomous navigation filters based on camera images. The IPB interfaces the navigation cameras and the on-board computer. IPB implement FPGA HW accelerators for the computer-vision algorithms used as part of the navigation filter and routes interfaces. The IPB embeds the **new European rad-hard FPGA from NanoXplore**. GMV will show our expertise using **NG-MEDIUM** FPGA and recent preliminary utilization of **NG-LARGE** FPGA as target of VHDL applications.

- ## 4B- CoRA-MBAD: A Model-based Avionics Design Environment for HW/SW Co-Design

  Company: Politecnico Di Milano (IT)
  Speaker: Fabrizio FERRANDI

"Compact Reconfigurable Avionics – Model Based Avionics Design" (CoRA-MBAD) is a TRP R&D study funded by ESA.

The main objective of the MBAD activity is to develop a model based avionics design environment and process enabling the HW/SW Co-design at a high abstraction level, and intensively relying on automatic code generation to optimize the development and the performance of compact reconfigurable avionics.

The outcome of MBAD activity, called MBAD System, will be deployed on a reconfigurable data handling core containing a GR740 and a BRAVE NG-MEDIUM FPGA.

MBAD System relies on high-level synthesis of C code, either manually implemented or generated by Embedded Coder® from Simulink® models, so that components can be deployed on the FPGA in a transparent way for the user.

The presentation will provide user feedback on the usage of BRAVE NG-MEDIUM FPGA in the context of the CoRA-MBAD study.

- **4C- NG-Medium remote configuration**

  Company: ALTRAN (FR)
  Speaker: Vincent THIBAULT

This presentation is based on an application note to describe how to set up the different use cases specified by the CNES in reference document [RD1] for the distant configuration of the NanoXplore NG-Medium FPGA.

ABSTRACTS PART-5 / Prooducts

- ## 5A- High-Performance Strategic European Building Block

  Company: Airbus Defence & Space (FR)
  Speaker: Marion LE PENVEN

This presentation will put in perspective the DAHLIA SoC developed under H2020 contract by both ADS and TAS groups. It will explain why DAHLIA and NG-Ultra are so important for Space since this is strategic for European non-dependence as well as will be representative of future way of working.

- ## 5B- 1st European Space Computer Core: Fusio-RT

  Company: 3D-PLUS (SP)
  Speaker: Coralie DANG-FELLER

In order to load the bitstream into the NG Medium FPGA, a configuration memory is needed. Therefore, the perfect fit to ensure global high reliable system is to use 3D PLUS 128 Mb TMR NOR. Using such Triplicated Memory ensure SEU immunity and SEFI mitigation.
FUSIO RT Computer Core embeds both NG MEDIUM and configuration 128Mb NOR memory in a very small factor. It enables designers to have a ready to use rad tolerant Computer Core for a wide range a space applications.
In this presentation, we will also present an overview of hardware functions dealing with NG Medium FPGA, such as Power management, Development Kits/Tools available for a quick start prototyping with NG MEDIUM FPGAs and, to a greater degree, others NX FPGAs.

- ## 5C- Europonder: European High-Throughput Transponders

  Company: Spacechips (UK)
  Speaker: Rajan BEDI

Spacechips is pleased to announce Europonder: a range of two channel, high-throughput transponders containing exclusively European components to allow OEMs to supply payloads without any US-licensed or restricted technologies. Initially three Europonder products will be offered containing NanoXplore's NG-Medium, NG-Large and NG-Ultra FPGAs, to allow satellite and spacecraft manufacturers to prototype using fully-representative signal processing, power distribution and clocking. Qualified flight-grade versions of Europonder-M/L/U will also be offered allowing OEMs to procure European, space-grade high-throughput transponders. The architecture of the products will be presented with the Europonder-M/L transceivers available in 2020 to be followed by a version containing NanoXplore's NG-Ultra FPGA.

See you next 26 and 27/11/2019 at Noordwijk, NL!

Take care.

Joël

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