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DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 <u>Scope</u>. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 <u>PIN</u>. The PIN is as shown in the following example:



1.2.1 <u>RHA designator</u>. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 <u>Device type(s)</u>. The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	RH-PMICL1A	Radiation hardened integrated current limiter

1.2.3 <u>Device class designator</u>. The device class designator is a single letter identifying the product assurance level as follows:

	Device class	Device requirements documentation						
	Q or V		Certification and qualification to MIL-PRF-38535					
1.2.4	Case outline(s).	he case outline(s) are as designated in MIL-STD-1835 and as follows:						
	Outline letter	Descriptive designator	<u>Terminals</u>	Package style				
	Х	See figure 1	20	Flat pack <u>1</u> / <u>2</u> /				
				0 11 <i>1</i>				

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

 $\underline{1}$ Al2O3 ceramic header with pullback of 0.01 inch x 0.02 inch.

2/ The lid is connected to the seal ring (the pin 7 of the package).

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1.3 Absolute maximum ratings. 3/

Power supply (VCC)	0.3 V to +54 V
Analog input (ISNS+ / ISNS- / TMS+ / TMS- / UVLO)	0.3 V to (VCC + 0.3) V
Analog input (VD)	40 V to (VCC + 0.3) V
Analog output (COMP / HYS)	0.3 V to (VCC + 0.3) V
Analog output (TM / Vg)	40 V to (VCC + 0.3) V
Analog output (TON / TOFF)	0.3 V to +4.6 V
Analog input/output (I_REF)	0.3 V to +4.6 V
Digital input (SET_STS / SET_FLB)	0.3 V to (VCC + 0.3) V
Digital input (TC_OFF / TC_ON)	40 V to (VCC + 0.3) V
Digital output (STS)	40 V to (VCC + 0.3) V
Electrostatic discharge (ESD):	
Human body model (HBM)	2000 V
Maximum junction temperature (TJ)	150°C
Maximum storage temperature	65°C to +150°C
Maximum lead temperature (soldering 10 seconds)	260°C <u>4</u> /
Thermal resistance, junction-to-case (θJC)	40°C/W <u>5</u> /
1.4 <u>Recommended operating conditions</u> .	
1.4 <u>Recommended operating conditions</u> . Power supply (VCC)	10 V to 52 V
1.4 <u>Recommended operating conditions</u> . Power supply (VCC) Ambient operating temperature range (TA)	10 V to 52 V 55°C to +125°C
 1.4 <u>Recommended operating conditions</u>. Power supply (VCC) Ambient operating temperature range (TA) 1.5 <u>Radiation features</u>. 	10 V to 52 V 55°C to +125°C
 1.4 <u>Recommended operating conditions</u>. Power supply (VCC) Ambient operating temperature range (TA) 1.5 <u>Radiation features</u>. Maximum total dose available (high dose rate = 50 – 300 rad(Si/s)) 	10 V to 52 V 55°C to +125°C 100 krads(Si) 6/
 1.4 <u>Recommended operating conditions</u>. Power supply (VCC)	10 V to 52 V 55°C to +125°C 100 krads(Si) <u>6</u> /
 1.4 <u>Recommended operating conditions</u>. Power supply (VCC)	10 V to 52 V 55°C to +125°C 100 krads(Si) <u>6</u> / 100 krads(Si) <u>6</u> /
 1.4 <u>Recommended operating conditions</u>. Power supply (VCC)	10 V to 52 V 55°C to +125°C 100 krads(Si) <u>6</u> / 100 krads(Si) <u>6</u> /
 1.4 <u>Recommended operating conditions</u>. Power supply (VCC)	10 V to 52 V 55°C to +125°C 100 krads(Si) <u>6</u> / 100 krads(Si) <u>6</u> / ≤ 125 MeV/(mg/cm ²) <u>7</u> /
 1.4 <u>Recommended operating conditions</u>. Power supply (VCC)Ambient operating temperature range (TA) 1.5 <u>Radiation features</u>. Maximum total dose available (high dose rate = 50 – 300 rad(Si/s)) Maximum total dose available (low dose rate ≤ 10 mrad(Si/s)) Single event phenomenon (SEP): No SEL occurs at effective LET (see 4.4.4.2) SET observed at threshold LET (see 4.4.4.2) 	10 V to 52 V 55°C to +125°C 100 krads(Si) <u>6</u> / 100 krads(Si) <u>6</u> / ≤ 125 MeV/(mg/cm ²) <u>7</u> / > 10 MeV/(mg/cm ²) 7/
1.4 Recommended operating conditions. Power supply (VCC) Ambient operating temperature range (TA) 1.5 Radiation features. Maximum total dose available (high dose rate = $50 - 300 \operatorname{rad}(\operatorname{Si/s})$) Maximum total dose available (low dose rate $\leq 10 \operatorname{mrad}(\operatorname{Si/s})$) Single event phenomenon (SEP): No SEL occurs at effective LET (see $4.4.4.2$) SET observed at threshold LET (see $4.4.4.2$) (Saturated cross section = $1.4 \times 10^{-5} \operatorname{cm}^2$)	10 V to 52 V 55°C to +125°C 100 krads(Si) <u>6</u> / 100 krads(Si) <u>6</u> / ≤ 125 MeV/(mg/cm ²) <u>7</u> / > 10 MeV/(mg/cm ²) <u>7</u> /
1.4 Recommended operating conditions.Power supply (VCC)Ambient operating temperature range (TA)1.5 Radiation features.Maximum total dose available (high dose rate = $50 - 300 \operatorname{rad}(\operatorname{Si/s})$)Maximum total dose available (low dose rate $\leq 10 \operatorname{mrad}(\operatorname{Si/s})$)Single event phenomenon (SEP):No SEL occurs at effective LET (see 4.4.4.2)SET observed at threshold LET (see 4.4.4.2)(Saturated cross section = $1.4 \times 10^{-5} \operatorname{cm}^2$)	10 V to 52 V 55°C to +125°C 100 krads(Si) <u>6</u> / 100 krads(Si) <u>6</u> / ≤ 125 MeV/(mg/cm ²) <u>7</u> / > 10 MeV/(mg/cm ²) <u>7</u> /

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

- 4/ Distance not less than 1.5 mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
- 5/ Measured on 2s2p board as per standard JEDEC JESD51-7 in natural convection.
- 6/ The manufacturer supplying device type 01 has performed characterization testing in accordance with MIL-STD-883 method 1019 condition A (high dose rate = 50 300 rads(Si)/s and condition D (low dose rate = 10 mrads(Si)/s to a dose level of 100 krad(Si). Manufacturer also performed accelerated annealing 1.5X over test and observed no time dependent effects. The post-irradiation of HDR and LDR test parametric values falls within the specification limits as specified in Table IA. The radiation end points limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and D.
- <u>7</u>/ Heavy ion single event effects(SEE) test was performed at the Cyclotron facility at Université de Louvain (UCL) in Louvain-La-Neuve (Belgium) with an Xenon(Xe) ion beam exposed inside a vacuum chamber. No single event latch-up (SEL) was observed when Xenon (Xe) ions beam exposed with a fluence 1x10⁷ ions/cm² at an angle 60° with bias voltage 52 V and operating temperature 125°C corresponding to an effective LET of 125 MeV·cm²/mg; and Single event transient (SET) observed at threshold LET > 10 MeV/(mg/cm²). For more information on SEP test results, customers are requested to contact the manufacturer.

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2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits. MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings. MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://guicksearch.dla.mil.)

2.2 <u>Non-Government publications</u>. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC Solid State Technology Association

EIA/JEDEC 51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org).

2.3 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 <u>Item requirements</u>. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 <u>Case outline</u>. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 2.

3.2.3 <u>Block diagram</u>. The block diagram shall be as specified in figure 3.

3.2.4 <u>Radiation exposure circuit</u>. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 <u>Electrical performance characteristics and postirradiation parameter limits</u>. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 <u>Marking</u>. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 <u>Certification/compliance mark</u>. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 <u>Certificate of compliance</u>. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 <u>Certificate of conformance</u>. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

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Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ TA ≤ +125°C	Group A subgroups	Device type	Lir	nits	Unit
		unless otherwise specified			Min	Max	
Operating supply voltage	vcc	RGND = 0 Ω , (ICL_GND shorted to the BUS_GND)	1,2,3	01	8.5		V
Supply current, ON state	ICC_ON	VCC = 37 V, RGND = 11 k Ω	1,2,3	01		3	mA
Supply current, OFF state	ICC_OFF	VCC = 37 V, RGND = 11 kΩ	1,2,3	01		3	mA
VCC versus. GND internal clamp voltage	VZ	VCC = 37 V, RGND = 11 kΩ	1,2,3	01	13.5	16	V
Under-voltage lockout turn-ON threshold	TURN_ON	VCC = 37 V, R1 = 20 kΩ, R2 = 220 kΩ, RH =1.6 kΩ	1,2,3	01	28	32	V
Under-voltage lockout hysterisis	HST	VCC = 37 V, R1 = 20 kΩ, R2 = 220 kΩ, RH = 1.6 kΩ	1,2,3	01	1.6	2	V
Tele-command input voltage turn_ON	VTC_ON	VCC = 37 V, R1 = 20 kΩ, R2 = 220 kΩ, RH = 1.6 kΩ, ON mode	1,2,3	01	2	3.6	v
Tele-command input voltage turn_OFF	VTC_OFF	VCC = 37 V, R1 = 20 kΩ, R2 = 220 kΩ, RH = 1.6 kΩ, OFF mode	1,2,3	01	2	3.6	v
Gate voltage range, ON state	Vgate_ON	VCC = 37 V, R1 = 20 kΩ, R2 = 220 kΩ, RH = 1.6 kΩ, SET_STS high	1,2,3	01	24	26	v
Gate voltage range, OFF state	Vgate_OFF	VCC = 37 V, R1 = 20 kΩ, R2 = 220 kΩ, RH = 1.6 kΩ, SET_STS low	1,2,3	01	36.8	37.1	v
Voltage threshold with current limitation sense (Between INS+ and INS-)	VLIM	VCC = 37 V, R1 = 20 kΩ, R2 = 220 kΩ, RH = 1.6 kΩ, SET_STS high	1,2,3	01	0.09	0.11	v
Trip-ON time	TON	RI_REF = 120 kΩ, CON = 10 nF, COFF = 47 nF	9,10,11	01	1.1	1.4	ms
Trip-OFF time	TOFF	RI_REF = 120 kΩ, CON = 10 nF, COFF = 47 nF	9,10,11	01	100	140	ms
Tele-command minimum <u>3</u> / pulse time	Tpulse_ON	VCC = 37 V, R1 = 20 kΩ, R2 = 220 kΩ, RH = 1.6 kΩ, SET_STS low	9,10,11	01	30		μs
Tele-command minimum <u>3</u> / pulse time	Tpulse_OFF	VCC = 37 V, R1 = 20 kΩ, R2 = 220 kΩ, RH = 1.6 kΩ, SET_STS high	9,10,11	01	30		μs

TABLE IA. Electrical performance characteristics.

See footnotes at end of table.

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Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ TA ≤ +125°C	Group A subgroups	Device type	Lir	nits	Unit	
		unless otherwise specified			Min	Max		
Tele-command immunity <u>3</u> / pulse time	Tpulse_ON_ Noise	VCC = 37 V, R1 = 20 kΩ, R2 = 220 kΩ, RH = 1.6 kΩ, SET_STS low	9,10,11	01		10	μs	
Tele-command immunity <u>3</u> / pulse time	Tpulse_OFF _Noise	VCC = 37 V, R1 = 20 kΩ, R2 = 220 kΩ, RH = 1.6 kΩ, SET_STS high	9,10,11	01		10	μs	
Telemetry								
Telemetry output voltage, ON state	VTM	RSENSE = 100 m Ω , RTMS = 5 k Ω , RTM = 240 k Ω , ISENSE = 500 mA	1,2,3	01	2.2	2.6	V	
STS output voltage range, ON state	VSTS	RSTS= 51 kΩ	1,2,3	01	4.4	5.6	V	
Telemetry current voltage, OFF state	ITM	RSENSE = 100 m Ω , RTMS = 5 k Ω , RTM = 240 k Ω , ISENSE = 500 mA	1,2,3	01		5	μA	
STS output current range, OFF state	ISTS	RSTS = 51 kΩ	1,2,3	01		5	μA	
Delay time (from TC_ON to VOUT= 0 to 10%)	Delay	Latched OFF configuration	9,10,11	01	40	120	μs	
Rise time (VOUT= 10 to 90%)	Rise_Time	Latched OFF configuration	9,10,11	01	10	100	μs	
Fall time (VOUT= 90 to 10%)	Fall_Time	Latched OFF configuration	9,10,11	01	10	60	μs	
Storage (from TC_OFF to VOUT=10%)	Storage	Latched OFF configuration	9,10,11	01	20	110	μs	

 TABLE IA.
 Electrical performance characteristics
 - continued.

<u>1</u>/ Devices supplied to this drawing have been characterized through all levels M, D, P, L, R of irradiation. However, this device radiation end point limits for the noted parameters are guaranteed at RHA level R only for the conditions as specified in MIL-STD-883, method 1019, condition A and condition D. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, TA = +25°C.

2/ This SMD devices circuit function is an integrated current limiter and group A subgroups 4, 5, 6 (dynamic test) and subgroups 7, 8A, 8B (functional test) have not been tested because those subgroups are irrelevant to the Integrated Current Limiter devices functional characteristics.

3/ Go no go test.

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TABLE IB. <u>SEP test limits</u>. <u>1/ 2/ 3/</u>

Device type	Vcc =	Bias for Latch-up test	
	SET observed at threshold LET]	Maximum device cross section	VCC = 52 V No latch-up (SEL) occurs effective LET <u>4</u> /
01	LET > 10 MeV/(mg/cm ²)	1.4x 10 ⁻⁵ cm ²	LET ≤ 125 MeV/(mg/cm ²)

1/ For SEP test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

<u>3</u>/ Worst case temperature is TA = +125°C ± 10°C for SEL.

4/ Heavy ion single event effects (SEE) test was performed at the Cyclotron facility at Université de Louvain (UCL) in Louvain-La-Neuve (Belgium) with an Xenon(Xe) ion beam exposed inside a vacuum chamber. No single event latch-up (SEL) was observed when Xenon (Xe) ions beam exposed with a fluence 1x10⁷ ions/cm² at an angle 60° with bias voltage 52 V and operating temperature 125°C corresponding to an effective LET of 125 MeV/(mg/cm²); and Single event transient (SET) was observed at LET threshold > 10 MeV/(mg/cm²). For more information on SEP test results, customers are requested to contact the manufacturer.

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Case X – continued.

Symbol	Dimensions					Notes	
	Inches		Millimeters				
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum	
А	0.075		0.087	1.91		2.21	
b	0.015		0.019	0.38		0.48	
с	0.003		0.006	0.076		0.152	1
D	0.505		0.515	12.83		13.08	
E	0.275		0.285	6.99		7.24	
E2	0.199	0.205	0.211	5.05	5.21	5.36	
E3		0.037			0.95		
е	0.045		0.055	1.14		1.4	
L	0.25		0.370	6.35		9.39	
Q	0.010			0.25			2
S1		0.021			0.55		

NOTES:

Deviation from MIL-STD-1835 reference F-9, configuration B: .003" minimum instead of .004" minimum.
 Deviation from MIL-STD-1835 reference F-9, configuration B: .010" minimum instead of .026" minimum.

FIGURE 1. Case outline - continued.

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Device type		01	
Case outline		Х	
Terminal number	Terminal symbol	Туре	Description
1	SET_STS	Digital input	Configuration pin. If shorted to GND, the current limiter at power- up is OFF. If connected to V _{CC} , the current limiter at power-up is normally ON.
2	TC_OFF	Digital input	Telecommand interface input for OFF pulsed signal.
3	SET_FLB	Digital input	Configuration pin. If connected to VCC, the foldback mode is enabled.
4	TON	Analog output	Used to set the trip-off time T _{ON} . A capacitor C _{ON} is connected between this pin and GND.
5	TOFF	Analog output	Used to set the recovery time TOFF. This pin has double functionality. If the COFF capacitor is connected between this pin and GND, it sets the TOFF value in re-triggerable mode. If the pin is shorted to GND, the device is configured in latched mode.
6	I_REF	Analog input/output	Used to set the current reference. An external high-precision resistor is connected between this pin and GND in order to set the current reference.
7	GND	Power supply	Ground. Return of the bias current and zero- voltage reference for all internal voltages. Connected to the main bus ground through a decoupling resistor to operate in floating ground configuration.
8	VD	Analog input	Sense pin of the external metal oxide semiconductor field effect transistor (MOSFET) drain voltage used to detect current limitation. A small series resistor can be useful to reduce power dissipation.
9	STS	Digital output	Telemetry digital status. A resistor has to be connected between the pin and the main bus ground.
10	TMS+	Analog input	Non-inverting input of the telemetry circuit. An accurate external resistor shall be connected between ISNS+ and this pin in order to guarantee the requested accuracy on the output source current for the analog telemetry.

FIGURE 2. Terminal connections.

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Device type		01	
Case outline		Х	
Terminal number	Terminal symbol	Туре	Description
11	TMS-	Analog input	Inverting input of the telemetry circuit. An accurate external resistor shall be connected between ISNS- and this pin in order to guarantee the requested accuracy on the output source current for the analog telemetry.
12	ТМ	Analog output	Output source current for the analog telemetry. A resistor has to be connected between this pin and the main bus ground.
13	COMP	Analog output	Output pin for current limitation loop compensation.
14	Vg	Analog output	MOSFET gate driver output.
15	ISNS-	Analog input	Inverting input of the operational amplifier curren limitation loop. The pin is tied directly to the hot (negative) end of the external current sense resistor. Never leave this pin floating.
16	ISNS+	Analog input	Non-Inverting input of the operational amplifier current limitation loop. The pin is tied directly to the hot (positive) end of the external current sense resistor. Never leave this pin floating.
17	VCC	Power supply	Supply input voltage.
18	HYS	Analog output	External setting of the under voltage lockout (UVLO) hysteresis. A resistor has to be connected between the main bus and this pin.
19	TC_ON	Digital input	Telecommand interface input for ON pulsed signal.
20	UVLO	Analog input	External setting of the UVLO turn-on threshold. The pin has to be tied to the midpoint of a resisted divider that senses the supply voltage versus may bus ground.

FIGURE 2. <u>Terminal connections</u> - continued.

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4. VERIFICATION

4.1 <u>Sampling and inspection</u>. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 <u>Screening</u>. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

- 4.2.1 Additional criteria for device classes Q and V.
 - a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - b. Interim and final electrical test parameters shall be as specified in table IIA herein.
 - c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 <u>Qualification inspection for device classes Q and V</u>. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 <u>Conformance inspection</u>. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 <u>Group C inspection</u>. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 <u>Additional criteria for device classes Q and V</u>. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 <u>Group D inspection</u>. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

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Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,9	1,9
Final electrical parameters (see 4.2)	1,2,3, <u>2</u> / 9,10,11	1,2,3, <u>3</u> / <u>4</u> / 9,10,11
Group A test requirements (see 4.4)	1,2,3,9,10,11	1,2,3,9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,9,10,11	1,2,3, <u>3/ 4</u> / 9,10,11
Group D end-point electrical parameters (see 4.4)	1,2,3,9,10,11	1,2,3,9,10,11
Group E end-point electrical parameters (see 4.4)	1	1

TABLE IIA. Electrical test requirements. 1/

1/ This SMD devices circuit function is an integrated current limiter and group A subgroups 4, 5, 6 (dynamic test) and subgroups 7, 8A, 8B (functional test) have not been tested because those subgroups are irrelevant to the Integrated Current Limiter devices functional characteristics.

- 2/ PDA applies to subgroup 1 and 9.
- 3/ PDA applies to subgroups 1, 9, and Δ 's. 4/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table IA).

Parameters	Symbol	Device type	Min	Max	Units
Supply current, ON state	ICC_ON	01	-60	+60	μA
Supply current, OFF state	ICC_OFF	01	-60	+60	μA
Voltage threshold with current limitation sense	VLIM	01	-2.0	+2.0	mV

TARI E IIR	Burn-in	delta	narameters	T₄ = +25°C
	Duni-in	ucita	parameters.	IA - 123 0

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4.4.4 <u>Group E inspection</u>. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at TA = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 <u>Total dose irradiation testing</u>. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and condition D as specified herein.

4.4.4.1.1 <u>Accelerated annealing test</u>. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krad(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25° C $\pm 5^{\circ}$ C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 <u>Single event phenomena (SEP)</u>. When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (for example: $0^{\circ} \le$ angle $\le 60^{\circ}$). No shadowing of the ion beam due to fixturing or package related affects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be \geq 20 micron in silicon.
- e. The test temperature shall be +25°C for the transient measurements and the maximum rated operating temperature ± 10 °C for the latchup measurements.
- f. Bias conditions shall be VCC = VCC maximum for the latchup measurements.
- g. For SEL test limits, see Table IB herein.
- h. For SET test limits, see Table IB herein.

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5. PACKAGING

5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 <u>Record of users</u>. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 <u>Comments</u>. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 <u>Abbreviations, symbols, and definitions</u>. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 <u>Sources of supply for device classes Q and V</u>. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 <u>Additional information</u>. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

- a. RHA test conditions of SEP.
- b. Occurrence of single event latchup (SEL) ..
- c. Occurrence of single event transient (SET).

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A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	RH-PMICL1A	Radiation hardened integrated current limiter
<u>ce class designator</u> .		

A.1.2.3 Device

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

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A.1.2.4 <u>Die details</u>. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 <u>Die physical dimensions</u> .	
Die type	Figure number
01	A-1
A.1.2.4.2 Die bonding pad locations and electrical functions.	
<u>Die type</u>	Figure number
01	A-1
A.1.2.4.3 Interface materials.	
<u>Die type</u>	Figure number
01	A-1
A.1.2.4.4 Assembly related information.	
<u>Die type</u>	Figure number
01	A-1
A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for de	etails.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

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A.2 APPLICABLE DOCUMENTS.

A.2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings. MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

A.2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 <u>Item requirements</u>. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 <u>Design, construction and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 <u>Die bonding pad locations and electrical functions</u>. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 <u>Interface materials</u>. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 <u>Assembly related information</u>. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

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A.3.3 <u>Electrical performance characteristics and post-irradiation parameter limits</u>. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 <u>Electrical test requirements</u>. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 <u>Marking</u>. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 <u>Certification of compliance</u>. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 <u>Certificate of conformance</u>. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 <u>Sampling and inspection</u>. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 <u>Screening</u>. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

- a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.
- b. 100% wafer probe (see paragraph A.3.4 herein).
- c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 <u>Group E inspection</u>. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.1, and 4.4.2 herein.

A.5 DIE CARRIER

A.5.1 <u>Die carrier requirements</u>. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

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A.6 NOTES

A.6.1 <u>Intended use</u>. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 <u>Comments</u>. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 <u>Abbreviations, symbols, and definitions</u>. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 <u>Sources of supply for device classes Q and V</u>. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

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APPENDIX A APPENDIX A FORMS A PART OF SMD 5962-17211



Pad layout coordinates					
Pad symbol	X center	Y center	Pad symbol	X center	Y center
SET_STS	-140.100	+1031.375	TMS-	+122.550	-1077.425
TC_OFF	-611.700	+1031.375	ТМ	+626.875	-1077.425
SET_FLB	-946.675	+698.875	COMP	+992.675	-788.500
TON	-992.475	+399.400	VG	+992.675	-274.950
TOFF	-992.475	+137.850	ISNS-	+992.675	-92
I_REF	-992.475	-134.700	ISNS+	+992.675	+92
ICL_GND	-992.475	-439.675	VCC	+992.700	+515.275
VD	-992.475	-754.375	HYS	+992.700	+706.075
STS	-268.650	-1077.425	TC_ON	+634.725	+1031.375
TMS+	-62.8250	-1077.425	UVLO	+132.650	+1031.375

NOTE: Units are in µm

Die bonding pad locations and electrical functions

Die physical dimensions. Die size: 100 mils x 107 mils Die thickness: 375 μm (± 25 μm) or 15 mil (±1 mil)

Pad Size: 110 µm x 110 µm

Interface materials.

Top passivation: TEOS = 500 nm (\pm 50 nm) SiN = 550 nm (\pm 55 nm) Polymide = 6000 nm (\pm 1000 nm)

Backside metallization: bare silicon

Glassivation. Type: See top passivation Thickness: See top passivation

Substrate: Silicon

Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-08-21

Approved sources of supply for SMD 5962-17211 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962R1721101VXA	F8859	RHRPMICL1AK02V
5962R1721101VXC	F8859	RHRPMICL1AK01V
5962R1721101V9A	F8859	RHRPMICL1AD2V

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- <u>2</u>/ <u>Caution</u>. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE <u>number</u>

Vendor name and address

F8859

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