REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Revisions to Table IIA and Table IIB to accommodate class V additions. Added MBE functionality waveforms - glg	16-01-11	Charles Saffle
B	Correct error in two places in 1.3 for unit of measure. – llb	17-07-25	Charles F. Saffle
C	Add device types 03 and 04 and no source device types 01 and 02. Update: 1.5, 4.2.1d for additional screening, table IB, and table IIA footnote 6. Correct Figure 5. Update to current MIL-PRF-38535 requirements. – llb	19-08-23	James R. Eschmeyer

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C						
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28						

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

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DRAWING APPROVAL DATE
14-11-24

REVISION LEVEL
C

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, FOUR - 2MEG X 8-BIT or ONE - 8MEG X 8-BIT (64M), USER-CONFIGURABLE, RADIATION-HARDENED, MAGNETORESISTIVE RAM (MRAM), MULTICHIP MODULE (MCM)

SIZE	CAGE CODE	
A	**67268**	**5962-13207**

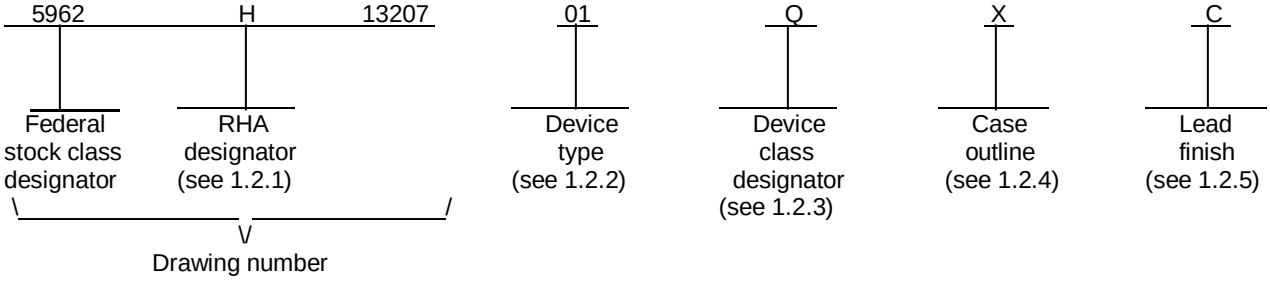
SHEET 1 OF 28

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	UT8MR8M8	8M X 8-bit rad-hard, user-configurable MRAM	50 ns
02	UT8MR8M8	8M X 8-bit rad-hard, user-configurable MRAM 1/	50 ns
03	UT8MR8M8	8M X 8-bit rad-hard, user-configurable MRAM 2/	50 ns
04	UT8MR8M8	8M X 8-bit rad-hard, user-configurable MRAM 1/ 2/	50 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	64	flat package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38535 for classes Q and V.

1/ Device types 02 and 04 provide QML Q product with additional testing as specified in paragraph 4.2.1d.
2/ Device types 03 and 04 include cold wafer probe as part of production flow.

1.3 Absolute maximum ratings. 1

Supply voltage range, (V_{DD})	-0.5 V dc to +4.3 V dc 2/
Voltage on any pin, (V_{IN})	-0.5 V dc to V_{DD} + 0.5 V dc 2/
Input/Output current, (I_{IO}) DC current per pin @ T_J = 125ºC for 20 years	± 20 mA
Power dissipation, P_D @ T_C = 105ºC	4.0 W 3/
Case temperature range, (T_C)	-40ºC to +105ºC
Storage temperature range, (T_{STG})	-65ºC to +125ºC
Junction temperature, (T_J)	+150ºC
Thermal resistance, junction-to-case, (θ_{JC}): Case X	5ºC/W
Magnetic field during write (H_{max_write})	8000 A/m
Magnetic field during read or standby (H_{max_read})	8000 A/m
Data retention (-40ºC to +105ºC)	20 years (minimum)
Endurance (-40ºC to +105ºC)	unlimited read/write cycles for 20 years

1.4 Recommended operating conditions. 2/

Operating supply voltage range, (V_{DD})	+3.0 V dc to +3.6 V dc
Supply voltage, (V_{SS})	0 V dc
Write inhibit voltage range, (V_{WI})	+2.5 V dc to +3.0 V dc 4/
Input high voltage, (V_{IH})	+2.0 V dc to +V_{DD}+0.3 V dc
Input low voltage, (V_{IL})	V_{SS} -0.3V to 0.8V
Case operating temperature range, (T_C)	-40ºC to +105ºC

1.5 Radiation features

Maximum total dose available (dose rate = 50 - 300 rad(Si)/s)	1 Mrads(Si) 5/
Single event phenomenon (SEP):	
No SEL occurs at effective LET (See 4.4.4.2)	≤ 112 MeV-cm^2/mg 6/
No SEU occurs at effective LET (See 4.4.4.2)	≤ 112 MeV-cm^2/mg 7/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltage values in this drawing are with respect to V_{SS}.
3/ Per MIL-STD-883, Method 1021.1, section 3.4.1, $P_D = (125°C - 105°C)/\theta_{JC}$.
4/ After power-up or if V_{DD} falls below V_{WI}, a waiting period of 2 ms must be observed, and $\overline{E}$ and $\overline{W}$ must remain high for 2 ms. Device is designed to prevent writing for all input conditions if V_{DD} falls below minimum V_{WI}.
5/ Device is irradiated at a dose rate = 50 – 300 rads (Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified.
6/ Test performed at V_{DD} = 3.6 V and at 125°C.
7/ Test performed at V_{DD} = 3.0 V and unpowered at 25°C.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Output load circuit. The output load circuit shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Radiation test circuit. The radiation test circuit shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request.

3.2.7 Functional tests. Various functional tests used to test this device are contained in the appendix A (herein). If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in Table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in Table IIA. The electrical tests for each subgroup are defined in Table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the specified temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.9 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process changes which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the specified temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-40°C \le T_C \le +105°C$ $+3.0\ V \le V_{DD} \le +3.6\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High-level input voltage	V_{IH}			1,2,3	All	2.0		V
Low-level input voltage	V_{IL}			1,2,3	All		0.8	V
High-level output voltage	V_{OH1}	I_{OH} = -4mA, $V_{DD} = V_{DD}$(min)		1,2,3	All	2.4		V
High-level output voltage	V_{OH2}	I_{OH} = -100µA, $V_{DD} = V_{DD}$(min)		1,2,3	All	V_{DD} - 0.2		V
Low-level output voltage	V_{OL1}	I_{OL} = 4mA, $V_{DD} = V_{DD}$(min)		1,2,3	All		0.4	V
Low-level output voltage	V_{OL2}	I_{OL} = 100µA, $V_{DD} = V_{DD}$(min)		1,2,3	All		V_{SS} + 0.2	V
Input capacitance 2/	C_{IN}	f = 1 MHz @ 0 V see 4.4.1e		4	All		50	pF
Bidirectional I/O capacitance 2/	C_{IO}			4	All		60	pF
Input leakage current	I_{IN}	$V_{IN} = V_{DD}$ and V_{SS}		1,2,3	All	-1	1	µA
Sleep/reset mode input leakage current,	I_{INZZ}	$V_{IN} = V_{DD}$ and V_{SS}		1,2,3	All	-0.25	0.25	mA
Three state output leakage current	I_{OZ}	$V_O = V_{DD}$ and V_{SS}, $V_{DD} = V_{DD}$ (max); $\overline{G}$ = V_{DD} (max)		1,2,3	All	-1	1	µA
Short-circuit output current 3/ 4/	I_{OS}	$V_{DD} = V_{DD}$ (max), $V_O = V_{DD}$, $V_O = V_{SS}$		1,2,3	All	-100	100	mA
Quiescent supply current	Q_{IDD}	CMOS leakage current ($\overline{E}$ = V_{DD}; all other inputs = V_{SS} or V_{DD}; V_{DD} = max)	-40°C +25°C	1,2,3	All		30	mA
			+105°C				35	
Deep power-down supply current 5/	Q_{IZZ}	CMOS leakage current ($\overline{E}$ = V_{DD}; all other inputs = V_{SS} or V_{DD}; V_{DD} = max)		1,2,3	All		1	mA
Active read supply current	I_{DDR}	Read mode, f = max (I_{OUT} = 0mA; V_{DD} = max)		1,2,3	All		140	mA
Active write supply current	I_{DDW}	Write mode, f = 10 MHz (V_{DD} = max)		1,2,3	All		140	mA
Functional test		See 4.4.1c, T_C = 25°C		7, 8A, 8B	All			

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-40^{o}C \leq T_C \leq +105^{o}C$ $+3.0\ V \leq V_{DD} \leq +3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AC Characteristics, Read Cycle 6/							
Read cycle time	t_{AVAV}	See figures 4 and 5 as applicable	9,10,11	All	50		ns
Address access time	t_{AVQV}		9,10,11	All		50	ns
Enable access time 7/	t_{ELQV}		9,10,11	All		50	ns
Output enable access time	t_{GLQV}		9,10,11	All		25	ns
Output hold from address change	t_{AXQX}		9,10,11	All	3		ns
Enable low to output active 8/	t_{ELQX}		9,10,11	All	3		ns
Output enable low to output active 8/	t_{GLQX}		9,10,11	All	0		ns
Enable high to output in high-Z 8/	t_{EHQZ}		9,10,11	All	0	15	ns
Output enable high to output in high-Z 8/	t_{GHQZ}		9,10,11	All	0	15	ns
AC Characteristics, $\overline{W}$ Controlled Write Cycle 9/							
Write cycle time 10/	t_{AVAV}	See figures 4 and 5 as applicable	9,10,11	All	50		ns
Address set-up time	t_{AVWL}		9,10,11	All	0		ns
Address valid to end-of-write ($\overline{G}$ high)	t_{AVWH}		9,10,11	All	28		ns
Address valid to end-of-write ($\overline{G}$ low)	t_{AVWH}		9,10,11	All	28		ns
Write pulse width ($\overline{G}$ high or low)	t_{WLWH} t_{WLEH}		9,10,11	All	28		ns
Data valid to end-of-write	t_{DVWH}		9,10,11	All	10		ns
Data hold time	t_{WHDX}		9,10,11	All	0		ns
Write low to data in high-Z 8/	t_{WLQZ}		9,10,11	All	0	15	ns
Write high to output active 8/	t_{WHQX}		9,10,11	All	3		ns
Write recovery time	t_{WHAX}		9,10,11	All	16		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-40^{o}C \le T_C \le +105^{o}C$ $+3.0\ V \le V_{DD} \le +3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AC Characteristics, $\overline{E}$ Controlled Write Cycle 9/							
Write cycle time 10/	t_{AVAV}	See figures 4 and 5 as applicable	9,10,11	All	50		ns
Address set-up time	t_{AVEL}		9,10,11	All	0		ns
Address valid to end-of-write ($\overline{G}$ high)	t_{AVEH}		9,10,11	All	28		ns
Address valid to end-of-write ($\overline{G}$ low)	t_{AVEH}		9,10,11	All	28		ns
Enable to end-of-write ($\overline{G}$ high) 11/	t_{ELWH} t_{ELEH}		9,10,11	All	28		ns
Enable to end-of-write ($\overline{G}$ low) 11/	t_{ELWH} t_{ELEH}		9,10,11	All	28		ns
Data valid to end-of-write	t_{DVEH}		9,10,11	All	10		ns
Data hold time 8/	t_{EHDX}		9,10,11	All	0		ns
Write recovery time 8/	t_{EHAX}		9,10,11	All	16		ns
AC Characteristics, Sleep Mode							
Sleep/reset mode exit delay 3/ 12/	t_{ZZL}	See figures 4 and 5 as applicable	9,10,11	All		100	µs
Sleep/reset mode access time 3/ 13/	t_{ZZH}		9,10,11	All	50		ns
Sleep/reset mode exit set-up time 3/	t_{EZZ}		9,10,11	All	0		ns
Sleep/reset mode settle time 3/	t_{ZZS}		9,10,11	All		200	µs

1/ Devices supplied to this drawing meet all levels M, D, P, L, R, F, G, and H of irradiation. However, these devices are only characterized at the "H" level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$

2/ This parameter is tested initially and after any design or process change which could affect this parameter, and therefore shall be guaranteed to the limits specified in Table IA.

3/ Guaranteed by design but not tested.

4/ Not more than one output may be shorted at a time, for a maximum duration of one second.

5/ Allow 100 µs to exit sleep/reset mode before performing any other operation and observe start-up time and start-up conditions for $\overline{W}$ and $\overline{E}$.

6/ $\overline{W}$ is high for read cycle. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read or write cycles.

7/ Address valid before or at the same time $\overline{E}$ goes low.

8/ Transition is measured at +/-400mV from the steady-state voltage.

9/ All writes occur during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state.

10/ All write cycle timings are referenced from the last valid address to the first transition address.

11/ If $\overline{E}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high-impedance state. If $\overline{E}$ goes high at the same time or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

12/ $\overline{W}$ and $\overline{E}$ must be high when ZZ/RST is pulled low in order to exit SLEEP/RESET mode.

13/ ZZ/RST must be high for 50ns in order to enter sleep mode.

Table IB. SEP test limits 1/ 2/

Device type	Single Event Upset (SEU) test 3/ V_{DD} = 3.0 V		Single Event Latch-up (SEL) test at bias V_{DD} = 3.6 V 4/
	Effective LET No SEU occurs	Maximum device Cross section	No SEL occurs at effective LET
All	LET ≤ 112 MeV/(mg/cm^2)	5/	LET ≤ 112 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.2 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Test temperature T_A = +25°C ±10°C.
4/ Worst case test temperature T_A = +125°C ±10°C.
5/ Tested to a LET of ≥ 112 MeV/(mg/cm^2) with no upsets.

Case outline X

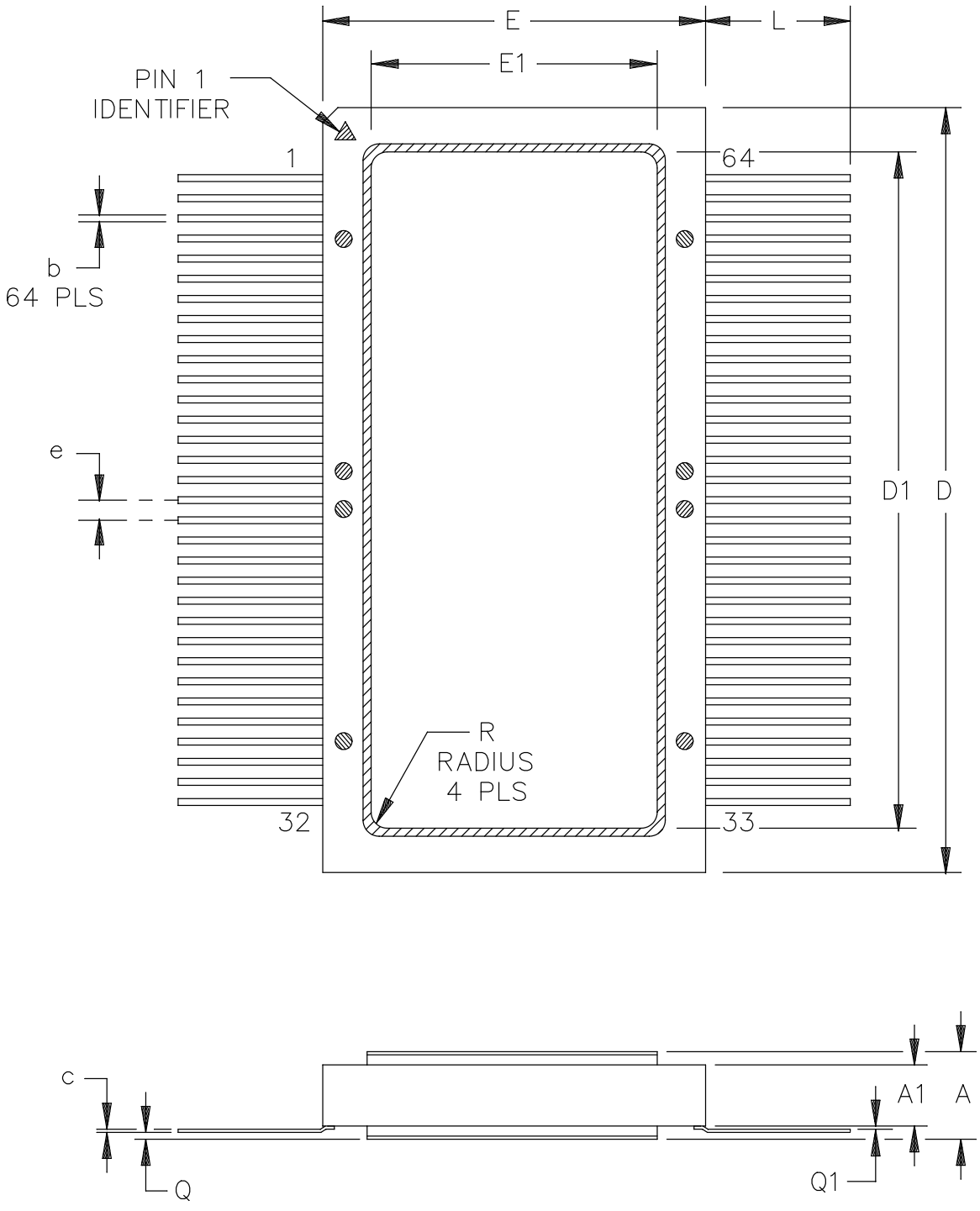


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-13207
DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990		REVISION LEVEL C	SHEET 10

Case outline X

Symbol	Inches	
	Min	Max
A		.238
A1	.136	.168
b	.015	.019
c	.004	.007
e	0.050 Typ.	
D	1.881	1.919
D1	1.663	1.697
E	.940	.960
E1	.702	.718
L	.290	.359
Q	.005 min	
Q1	.002	.014
R	0.034 Typ.	

NOTES:
1. All exposed metal and metalized areas shall be gold plated per MIL-PRF-38535.
2. The seal ring and lids are electrically connected to V_{SS}.
3. Dogleg geometries optional within dimensions shown.
4. Lead finish is in accordance with MIL-PRF-38535.
5. Tie bar may have excise slots of various configurations and are vendor option. Tie bar dimensions are for reference only.
6. Package material: opaque 90% minimum Alumina ceramic.
7. ESD classification mark or dot is located in the pin 1 corner within area shown.

FIGURE 1. Case outline - Continued.

Case X

Device type	All	Device type	All
Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	VSS	33	VSS
2	VDD	34	VDD
3	VSS	35	VSS
4	VSS	36	VSS
5	$\overline{E0}$	37	A14
6	A4	38	A13
7	A3	39	A12
8	A2	40	A11
9	A1	41	A10
10	A0	42	$\overline{W}$
11	A19	43	MBE
12	ZZ/RST	44	VSS
13	NUO	45	$\overline{E2}$
14	DQ4	46	DQ0
15	DQ5	47	DQ1
16	VDD	48	VDD
17	VSS	49	VSS
18	DQ6	50	DQ2
19	DQ7	51	DQ3
20	$\overline{E1}$	52	VSS
21	$\overline{E\_All}$	53	$\overline{G}$
22	A21	54	VSS
23	A22	55	A18
24	A9	56	A17
25	A8	57	A16
26	A7	58	A15
27	A6	59	A20
28	A5	60	$\overline{E3}$
29	VSS	61	VSS
30	VSS	62	VSS
31	VSS	63	VSS
32	VDD	64	VDD

FIGURE 2. Terminal connections.

Chip Enable Functions Table

$\overline{E\_All}$	$\overline{E0}$	$\overline{E1}$	$\overline{E2}$	$\overline{E3}$	A22	A21	Comment
0	1	1	1	1	0	0	MRAM Die 0 Enabled
0	1	1	1	1	0	1	MRAM Die 1 Enabled
0	1	1	1	1	1	0	MRAM Die 3 Enabled
0	1	1	1	1	1	1	MRAM Die 2 Enabled
1	0	1	1	1	X	X	MRAM Die 0 Enabled
1	1	0	1	1	X	X	MRAM Die 1 Enabled
1	1	1	0	1	X	X	MRAM Die 2 Enabled
1	1	1	1	0	X	X	MRAM Die 3 Enabled

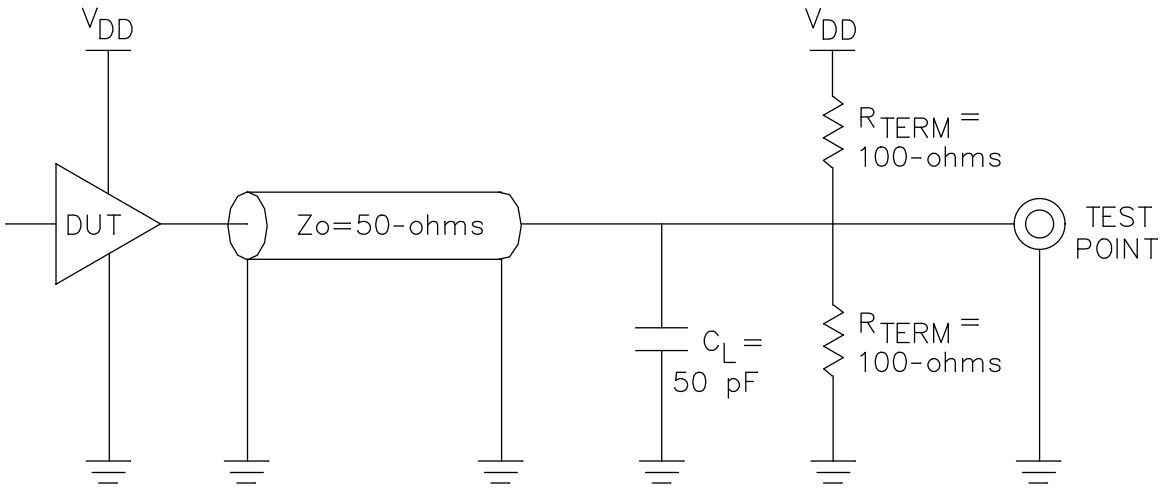
Note : Only one $\overline{E}$[3:0] pin may be active at any given time.

Device Operation Truth Table

ZZ/RST	$\overline{E}$ [3:0]	$\overline{G}$	$\overline{W}$	Mode	V_{DD} Current	DQ[7:0]
H	X	X	X	Deep Sleep/Reset Mode	Q_{IZZ}	Hi-Z
L	H	X	X	Not Selected	Q_{IDD}	Hi-Z
L	L	H	H	Output Disabled	I_{DDR}	Hi-Z
L	L	L	H	Byte Read	I_{DDR}	D_{OUT}
L	L	X	L	Byte Write	I_{DDW}	D_{IN}

Note: Only one $\overline{E}$[3:0] pin may be active at any given time.

FIGURE 3. Truth table.



Notes: 1. 50 pF including scope probe and test socket.
2. Measurement of data output occurs at the low to high or high to low transition mid-point, typically, $V_{DD}/2$.

FIGURE 4. Output load circuit

Power up and power down sequencing diagram

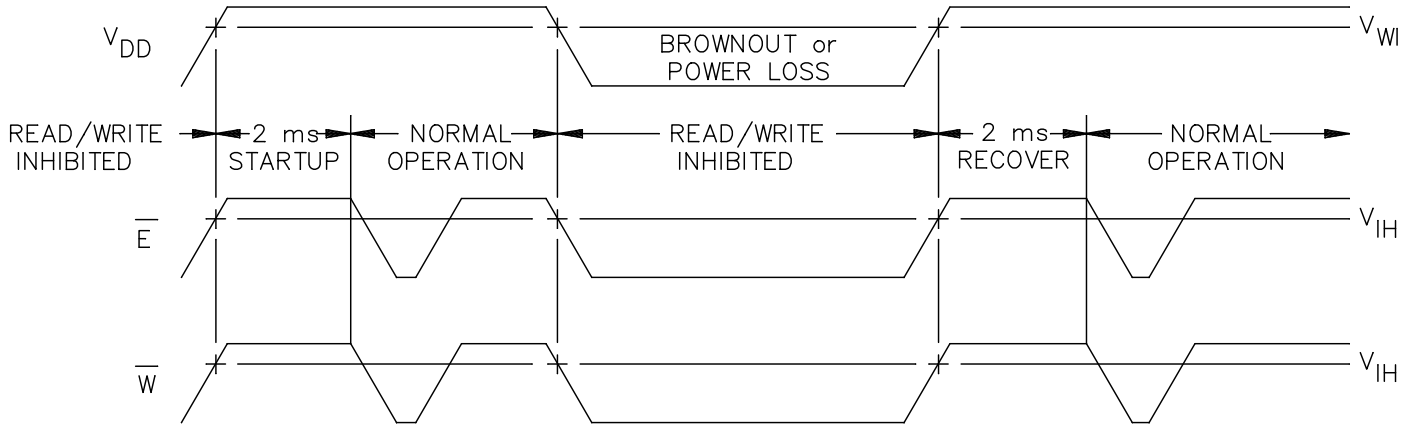
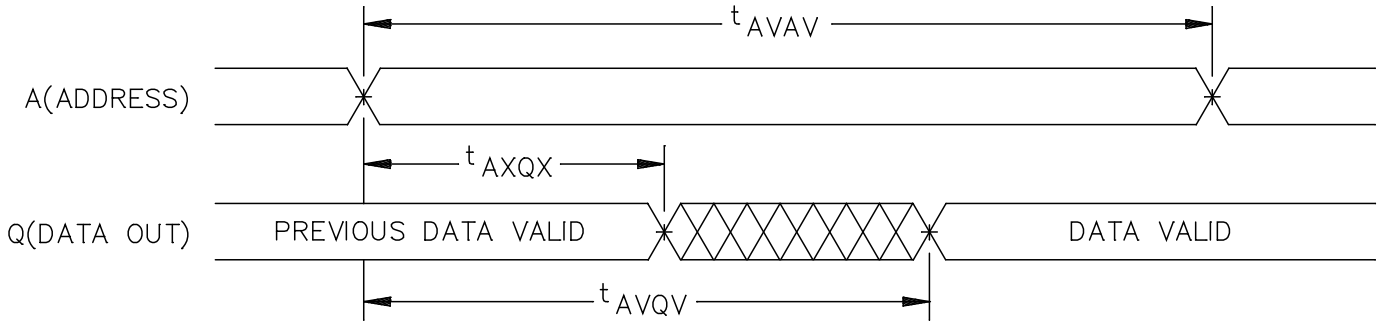


FIGURE 5. Timing waveforms.

MRAM read cycle 1: Address Access



Note: Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

MRAM read cycle 2: Chip enable Access

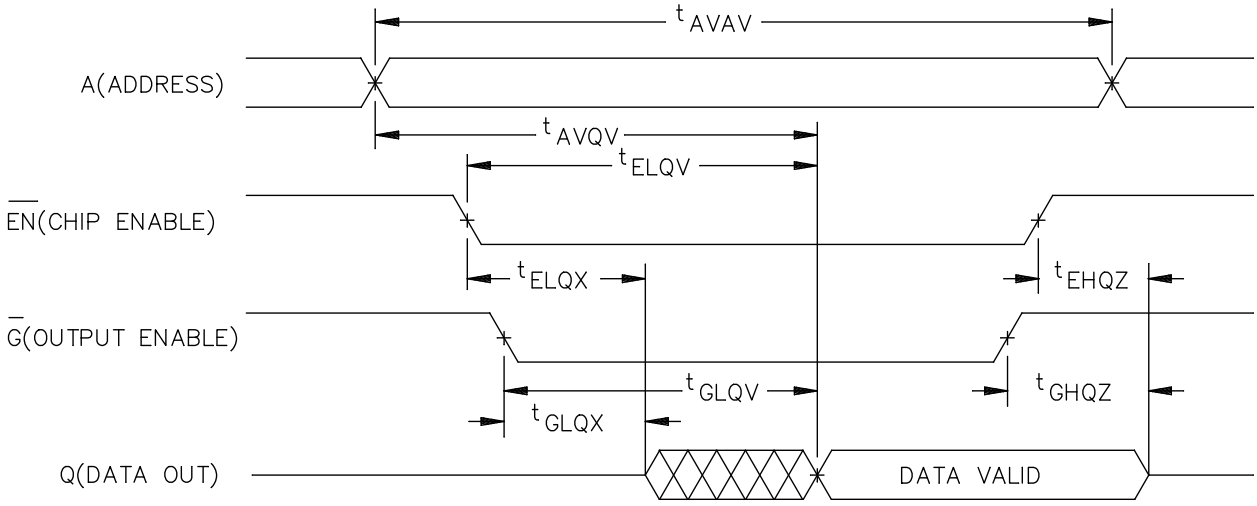


FIGURE 5. Timing waveforms - Continued.

MRAM Write Cycle 1: $\overline{W}$ Controlled Access

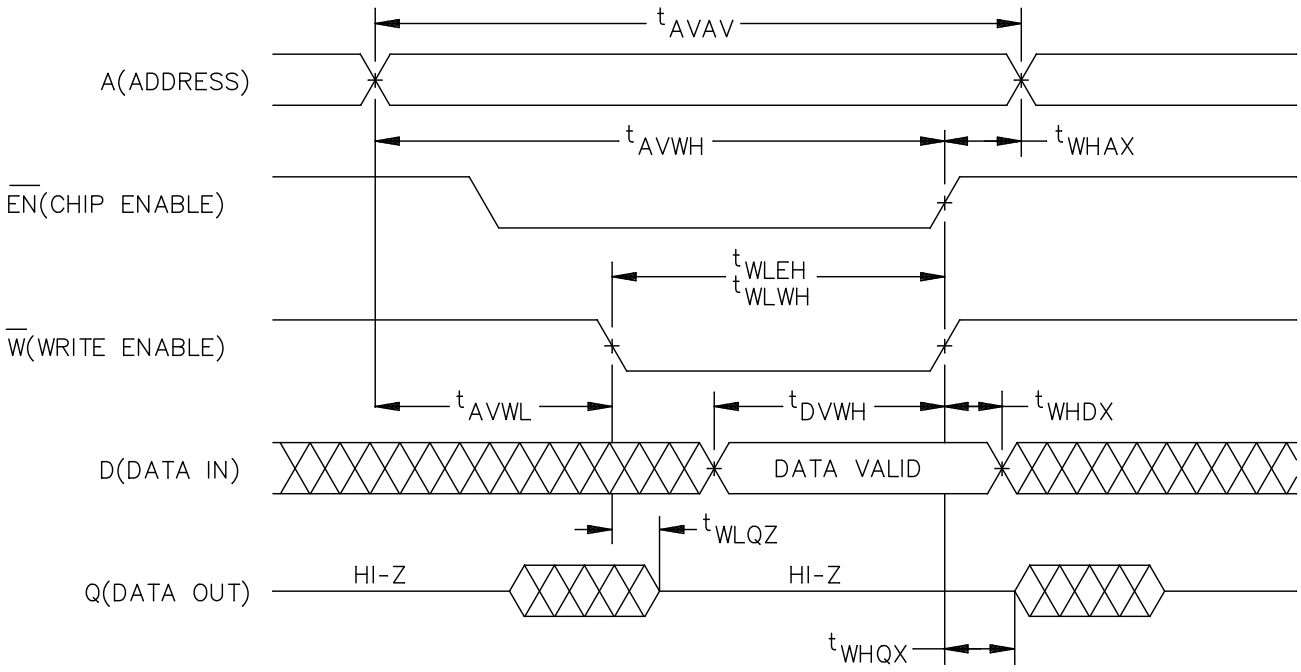


FIGURE 5. Timing waveforms - Continued.

MRAM Write Cycle 2: $\overline{E}$ Controlled Access

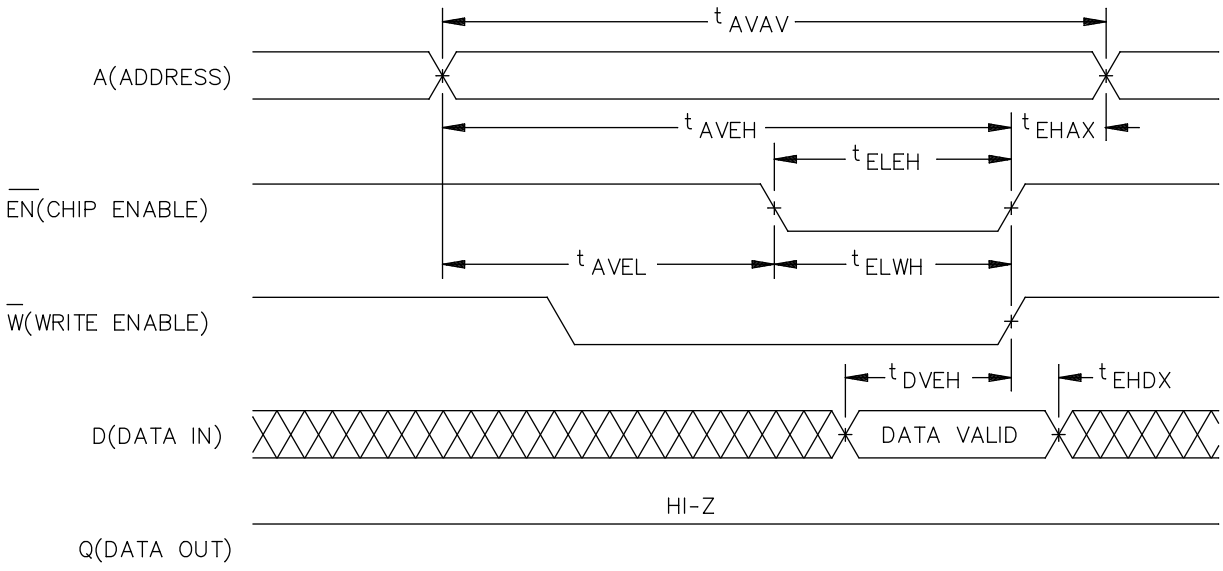


FIGURE 5. Timing waveforms - Continued.

MRAM Sleep Mode Timing Diagram

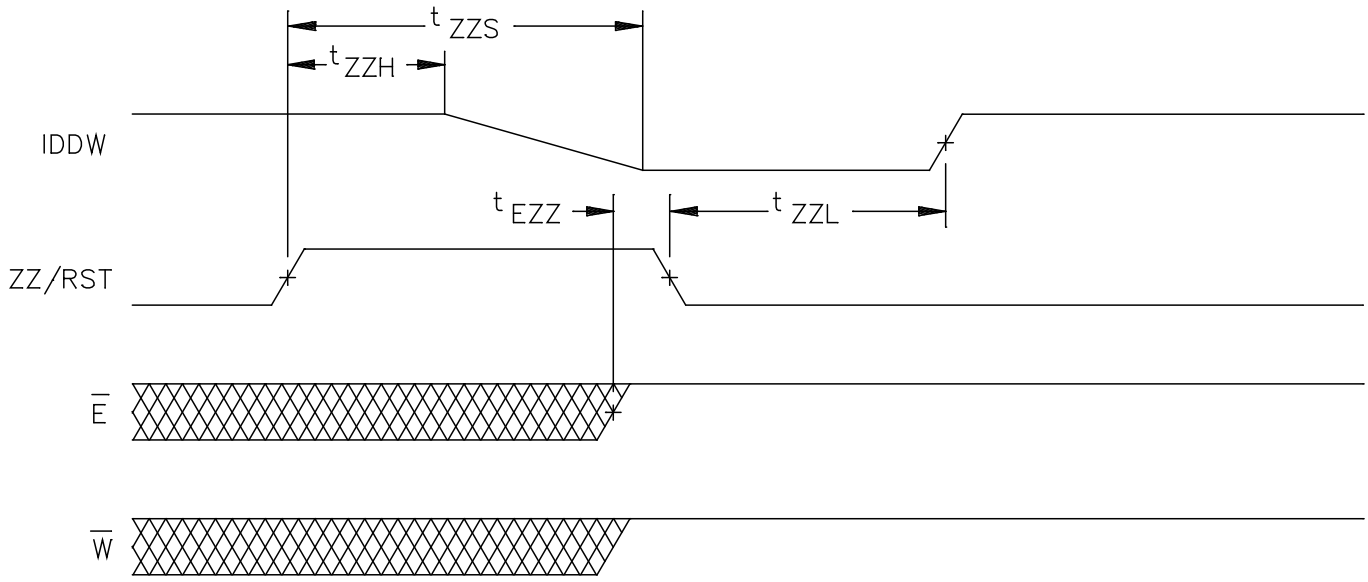


FIGURE 5. Timing waveforms - Continued.

MBE Functionality: Accessing Individual Die via $\overline{E}$_ALL and A[22:21]

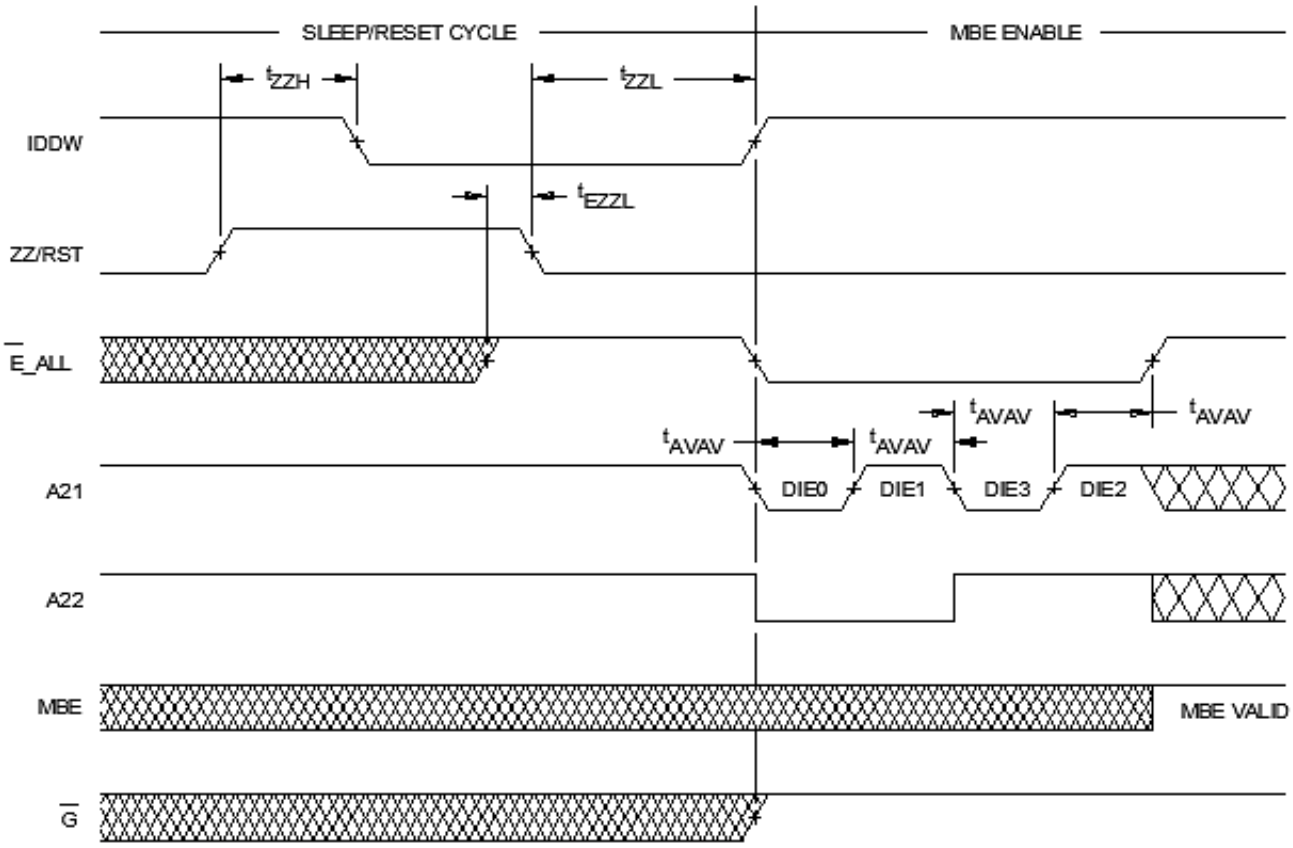


FIGURE 5. Timing waveforms - Continued.

MBE Functionality: Accessing Individual Die via $\overline{E}$[3:0]

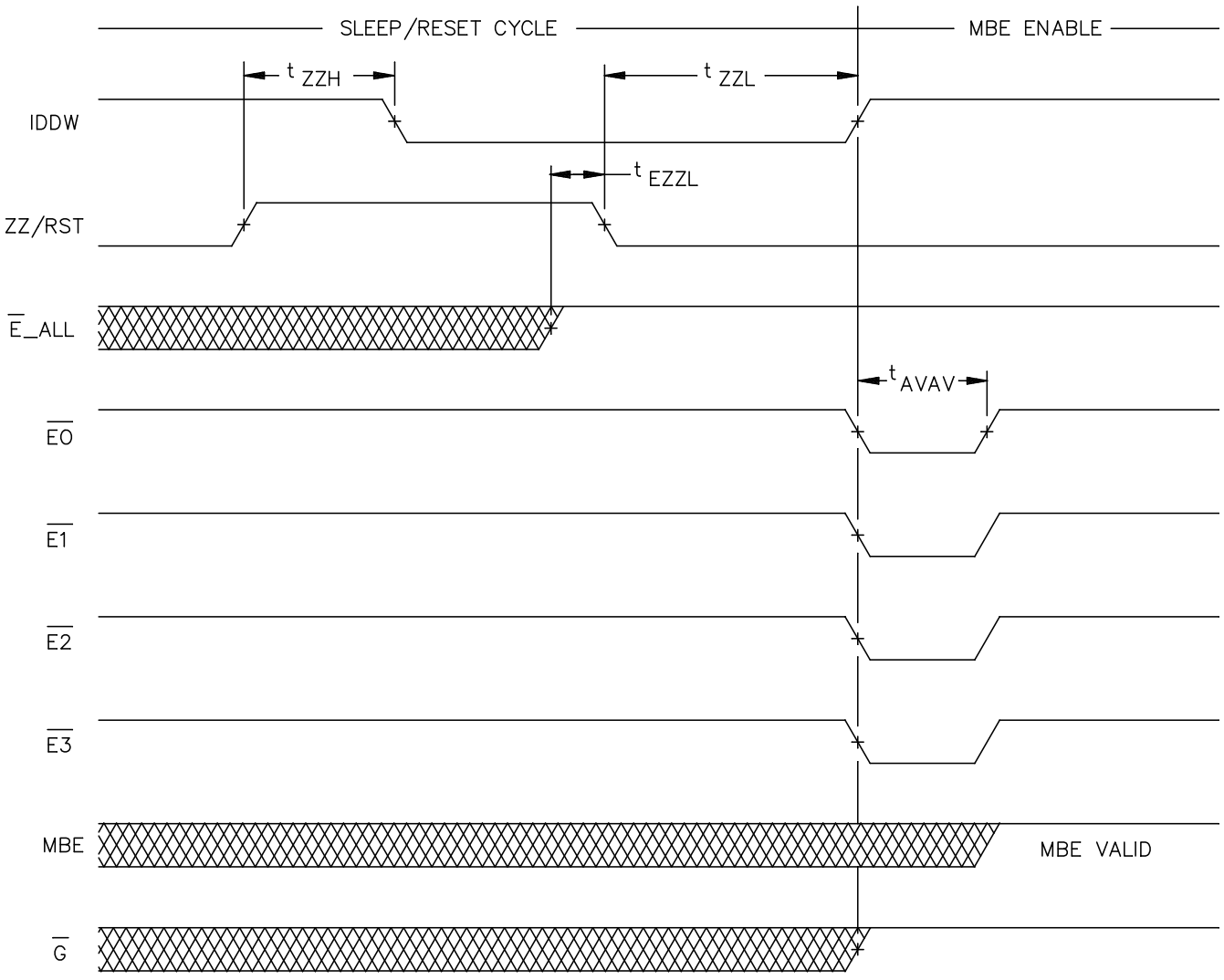


FIGURE 5. Timing waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

d. Additional screening for device types 02 and 04.

(1) 100% internal visual, method 2010 condition A of MIL-STD-883.

(2) 100% PIND (Single pass).

(3) Serialization.

(4) 100% X-ray (Top view only).

(5) Group A.

(6) Dynamic burn-in at +125ºC for 240 hours or equivalent and static burn-in at +125°C for 144 hours (device type 04 only method 1015 of MIL-STD-883), deltas, PDA (3%) for Functional Test only, and PDA (10%) for DC and Functional Test combined.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1*, 2, 3, 4**, 5, 6, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 4**, 5, 6, 7*, 8A, 8B, 9, 10, 11
2	Static burn-in I and II (method 1015)	Not required	Required
3	Same as line 1	Not required	1*, 4**, 7*, 9 Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1	1*, 4**, 7*, 9 Δ	1*, 4**, 7*, 9 Δ
6	Final electrical parameters	1*, 2, 3, 4**, 5, 6, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 4**, 5, 6, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements	1, 2, 3, 4**, 5, 6, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 5, 6, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters	1, 2, 3, 4**, 5, 6, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 5, 6, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters	1, 2, 3, 4**, 5, 6, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 5, 6, 7, 8A, 8B, 9, 10, 11
10	Group E end-point electrical parameters	1, 4**, 7, 9	1, 4**, 7, 9

1/ Blank spaces indicates tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify functionality of the device.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see Table IIB) shall be required where specified, and the delta values shall be computed with reference to previous interim electrical parameters (see Line 1). For device class V, and device class Q, device types 02 and 04, performance of delta limits shall be specified in the manufacturer's QM plan.
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25ºC.

Parameter 1/	Limit	Unit
Supply current standby at 0 MHz, Q_{IDD}	± 3.0 mA of previous measured value	mA
Deep power-down and reset supply current, Q_{IZZ}	± 50 µA of previous measured value	µA
Input leakage current, I_{IN}	± 50 nA of previous measured value	nA
Input leakage current (sleep/reset mode), I_{INZZ}	± 2 µA of previous measured value	µA
Low-level input voltage, V_{IL}	± 250 mV of previous measured value	mV
High-level input voltage, V_{IH}	± 150 mV of previous measured value	mV

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.1 Group A inspection.

a. Tests shall be as specified in Table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device.

d. O/V (Latch up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device classes Q and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in Table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in Table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535 and the end-point electrical parameters shall be as specified in Table IIA herein.

a. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the post-irradiation end-point electrical parameter limits as defined in Table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in Table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in Table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5ºC. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. ASTM standard F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^{o} \leq$ angle $\leq 60^{o}$). No shadowing of the ion beam due to fixturing or package related effects are allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^{7}$ ions/cm^{2}.

c. The flux shall be between 10^{2} and 10^{5} ions/cm^{2}/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be > 20 microns in silicon.

e. The test temperature shall be +25ºC ±10ºC for single event upset testing and at the maximum rated operating temperature +10ºC for single event upset testing.

f. Bias conditions shall be defined by the manufacturer for latch-up measurements.

g. Test four devices with zero failures.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions.(SEP).

b. Number of upsets (SEU).

c. Occurrence of latchup (SEL).

APPENDIX A

Appendix A forms a part of SMD 5962-13207

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-08-23

Approved sources of supply for SMD 5962-13207 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/ 4/	Vendor CAGE number	Vendor similar PIN 2/
5962H1320701QXC	3/	UT8MR8M8-50XQC
5962H1320701VXC	3/	UT8MR8M8-50XVC
5962H1320702QXC	3/	UT8MR8M8-50XQC
5962H1320703QXC	65342	UT8MR8M8-50XQC
5962H1320704QXC	65342	UT8MR8M8-50XQC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

4/ Device types 03 and 04 are the direct replacement part of device types 01 and 02 respectively. However device types 03 and 04 have been tested at cold wafer probe as part of production flow.

Vendor CAGE number	Vendor name and address
65342	Cobham Colorado Springs, Inc. 4350 Centennial Blvd. Colorado Springs, CO 80907-3486

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.