Influence of assembly methods and thermal cycling on MLCC capacitors on crack appearance. Microsection study

C. López-López, *E. Torres,S. Reina,C. Marcos, M. Dominguez, J.M. Jimenez*

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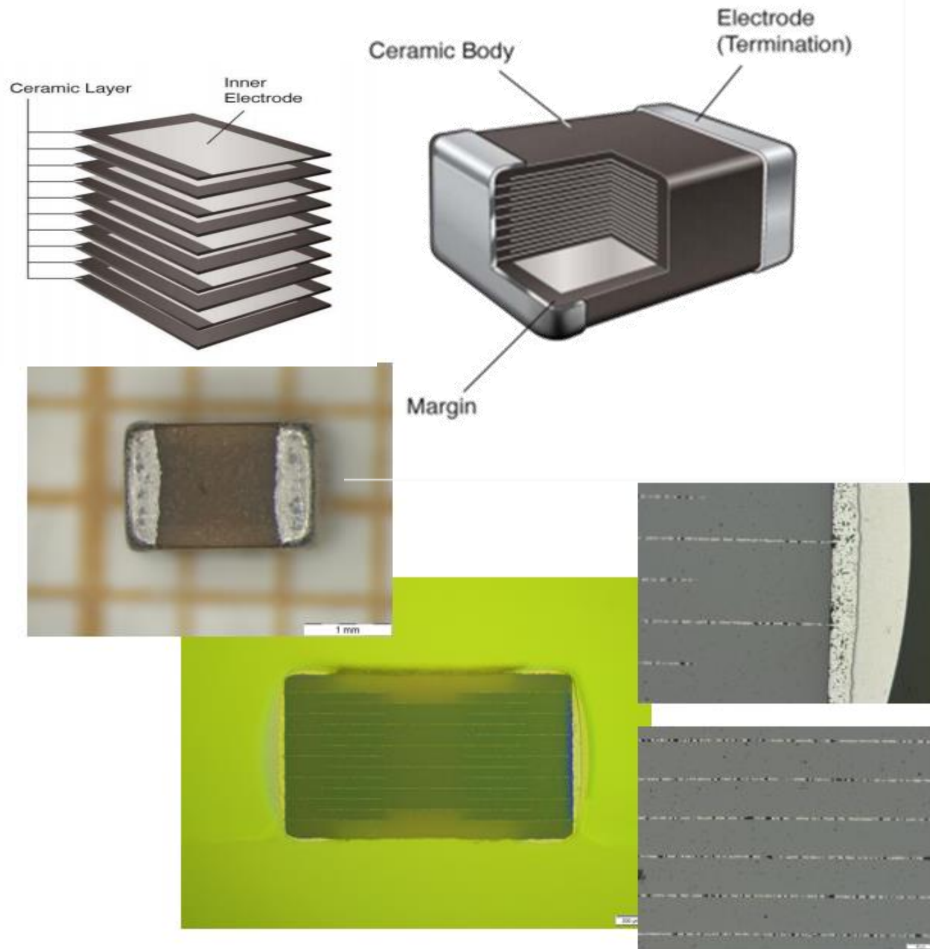
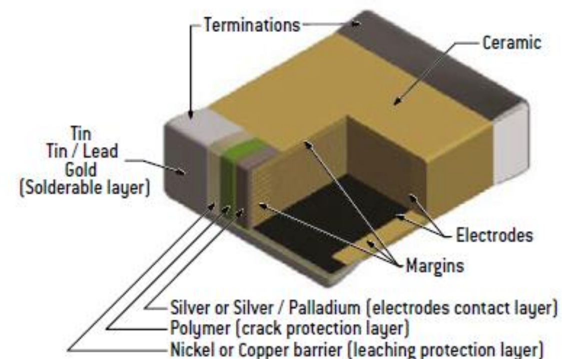
Multilayer Ceramic Capacitors



- Ceramic capacitors are the most widely used passive component in electronic circuit .
- MLCCs are composed of dielectric layers, inner electrodes, and outer terminal electrodes.
- Some MCLL designs add Flexible Terminations to improve the performance of the device.



T. Tsurumi & T. Hoshina, .Handbook of Advanced Ceramic, 2013, 415-427
MJ Pan & CA Randall, IEEE Electrical Insularion Magazine, 26 (3), 2010, 44-50.

J. Prymark et al., CARTS USE Proceedings, 29 Passive Components Symposium, 2009.

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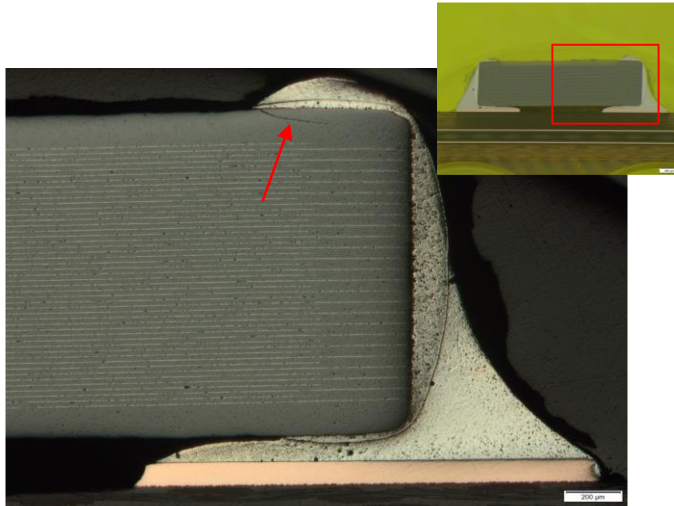
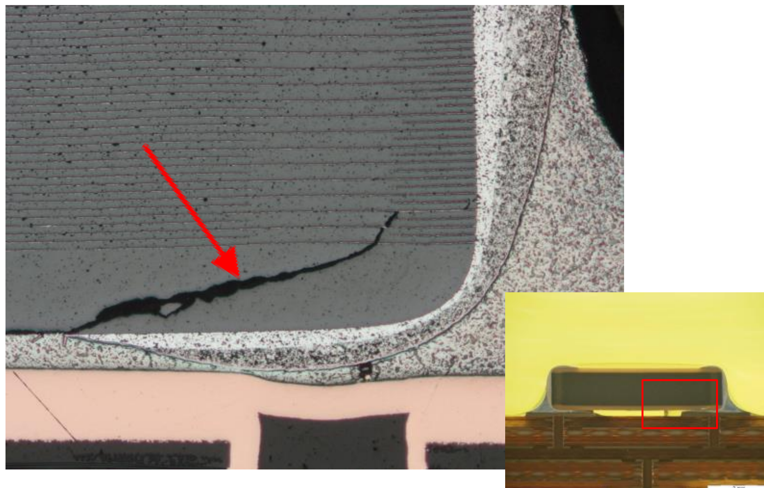
Fracture failure on assembled Multilayer Ceramic Capacitors





Cracking is related mostly to the thermal or mechanical stress caused during:

- **Handling**
- **Assembly**
- **Testing**

Some factors that influence on the appearance of cracks during the **assembly process** are:

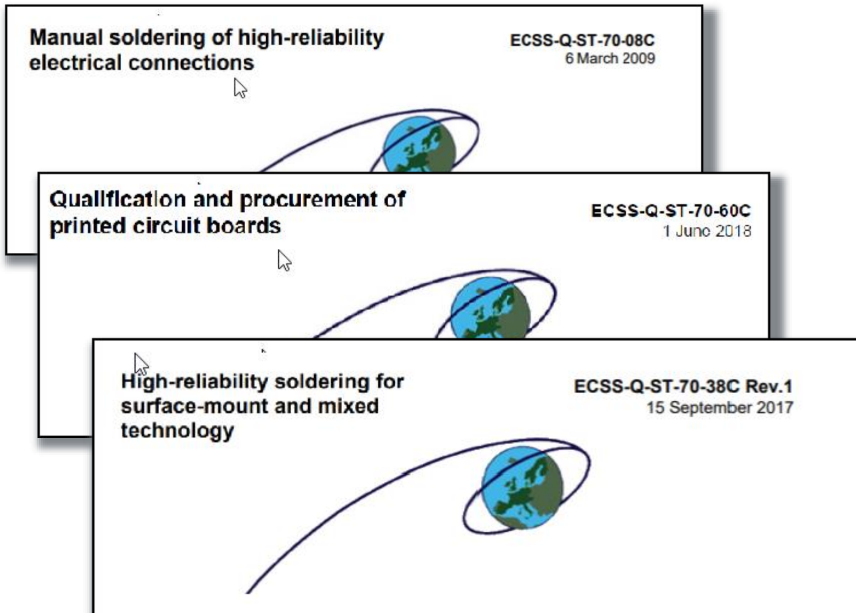
- Excessive volume of solder
- Impact by mounting machine
- Incorrect heating and cooling process
- Deflexion of sustrate

A. Teverovsky, NASA Technical report, ID.20190001592, 2019.
B. J.AlAhmar, E. Wiss, S. Wiese, IEEE, EurosimE, 2018.

INTRODUCTION

Verification Procedure

- The soldering verification is performed according to ECSS-Q-ST-70-38C Rev.1, 10C, -12C, -08C, -60C.



- The standards defines the <u>technical</u> requirements and <u>quality</u> assurance provisions

ECSS-Q-ST-70-38C Rev.1
15 September 2017

14.3 Verification programme

a. The verification programme as shown in Figure 14-1 shall consist of:

1. Visual inspection in conformance with clause 13.
2. Vibration and shock testing in conformance with clause 14.5.
3. Temperature cycling in conformance with clause 14.6 except for area array devices .
4. Microsectioning in conformance with clause 14.7.

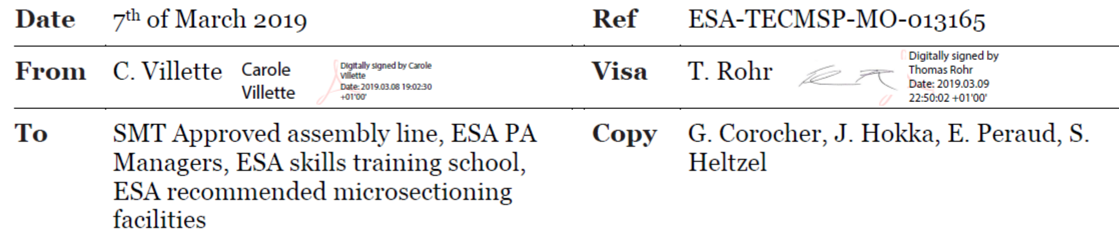
- To carry out the microsection the lab have to be certify by the ESA

INTRODUCTION

Verification Procedure

MEMO

ESA-TECMSP-MO-013165



Date	7th of March 2019	Ref	ESA-TECMSP-MO-013165
From	C. Villette Carole Villette (Digitally signed by Carole Villette Date: 2019.03.08 19:02:30 +01'00')	Visa	T. Rohr (Digitally signed by Thomas Rohr Date: 2019.03.09 22:50:02 +01'00')
To	SMT Approved assembly line, ESA PA Managers, ESA skills training school, ESA recommended microsectioning facilities	Copy	G. Corocher, J. Hokka, E. Peraud, S. Heltzel

Subject: ESA recommended microsectioning facilities

The following facilities are ESA recommended for inspection, microsectioning and assessment of the microsectioning of assembled devices mounted on verification boards, having been submitted to a verification programme in compliance with ECSS-Q-ST-70-07C, ECSS-Q-ST-70-08C and ECSS-Q-ST-70-38C.

The competencies of the laboratories have been assessed by ESA in compliance with ESA-TECMSP-MO-013161 (www.escies.org). These companies are considered as Category A as described in the ESA-TECMSP-MO-013162 (www.escies.org).

These companies may also provide expertise in the field of unpopulated Printed Circuit Board microsectioning.

The list of companies is uploaded on the escies website (www.escies.org).

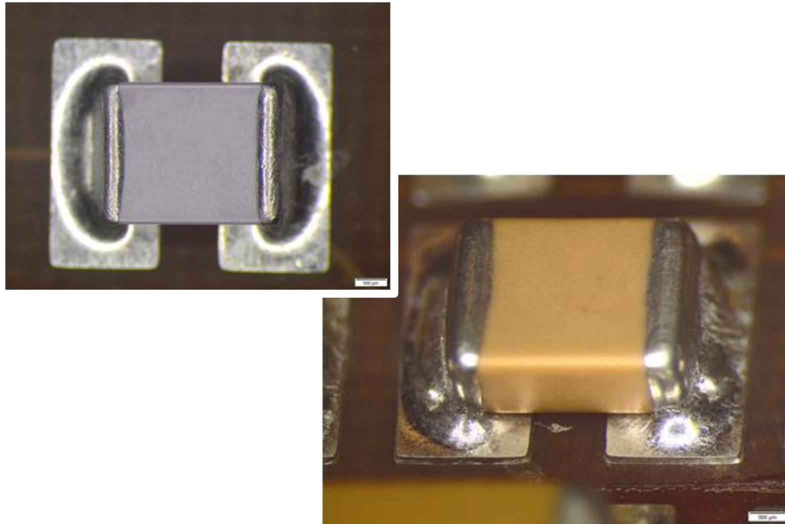
Alter Technology TUV

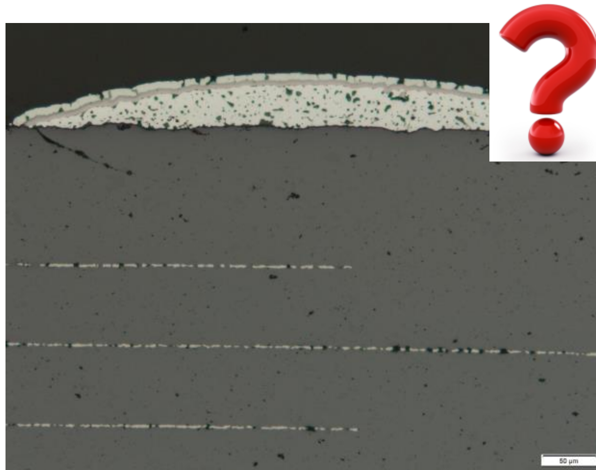
Mr. Manuel Dominguez

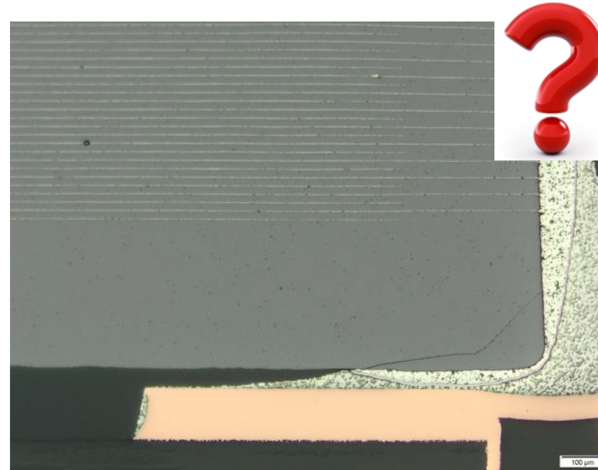
GOALS

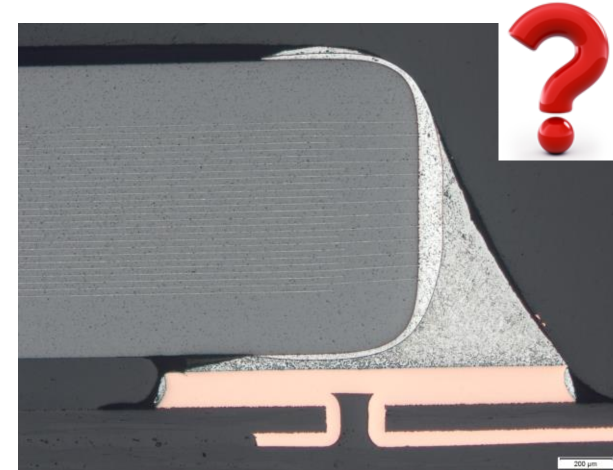
The aim of this study is to asses the susceptibility to cracking of soldered MLCC capacitors, as a function of:

- Manufacturer
- Assembly method
- Dielectric Type
- Thermal cycling conditions









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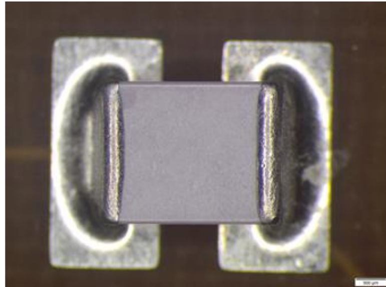

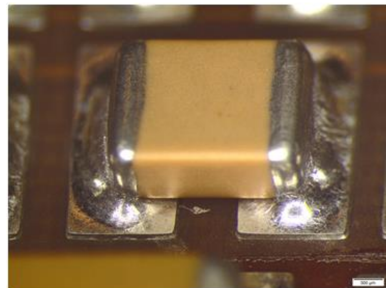

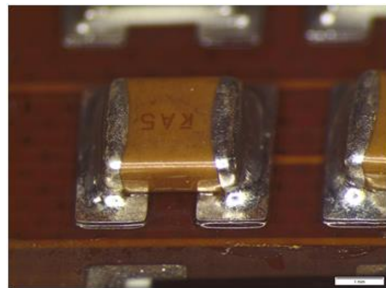

Ceramic Capacitor Size 1210

- Manufacturer
  - MFR1
  - MFR2
  - MFR3
  - MFR4 (flex Termination)
- Mounting Process
  - **VP**: Vapor Phase
  - **HS1**: Hand Soldering I
  - **HS2**: Hand Soldering II
- Dielectric Type
  - Type I
  - Type II
- Thermal Cycling Ramp1>Ramp2

! Due to the large number of possible combinations this study will be performed on **52** devices

EXPERIMENTAL PROCEDURE

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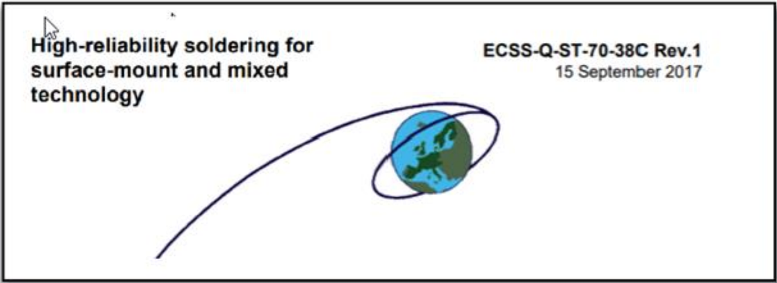
TEST FLOW

Visual Inspection & Photos → Vibration → Visual Inspection & Photos → 135 Thermal Cycles -55C/100C Ramp2 → Visual inspection & Photos → 365 Thermal Cycles -55C/100C
- Ramp1
- Ramp2

→ Visual Inspection & Photos → Microsections



EXPERIMENTAL PROCEDURE

Test Flow

External Visual Inspection

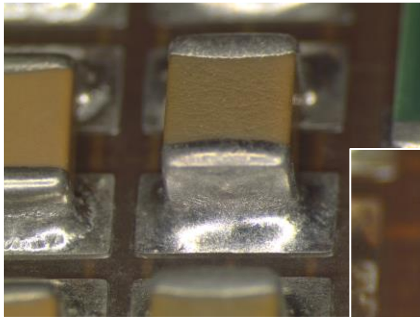
High-reliability soldering for surface-mount and mixed technology

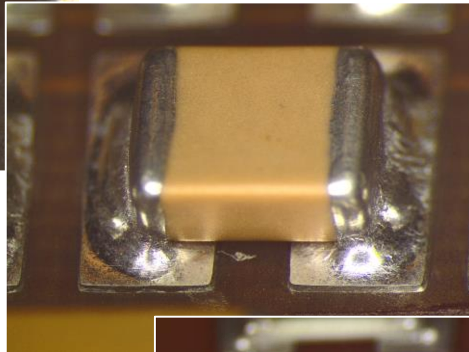
ECSS-Q-ST-70-38C Rev.1
15 September 2017

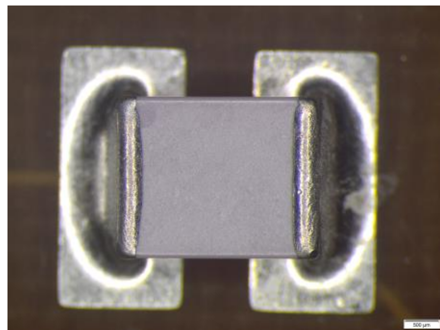
13.3 Visual rejection criteria

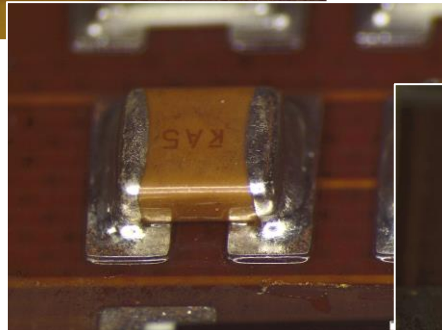
a. The following are some characteristics of unsatisfactory conditions, any of which shall be cause for rejection:

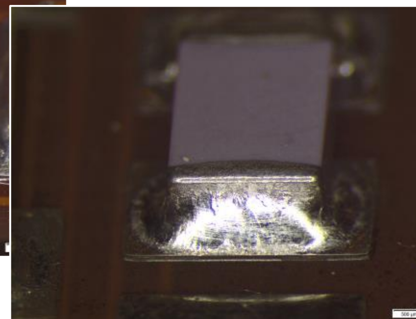
1. charred, burned or melted insulation of devices,
2. conductor pattern separation from circuit board,
3. burns on base materials,
4. <<deleted>>
5. excessive solder (including peaks, icicles and bridging), see clause 11.5,
6. flux residue, solder splatter, solder balls, or other foreign matter on circuitry, beneath devices or on adjacent areas,
7. dewetting,

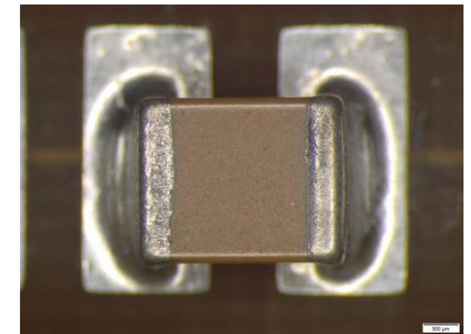






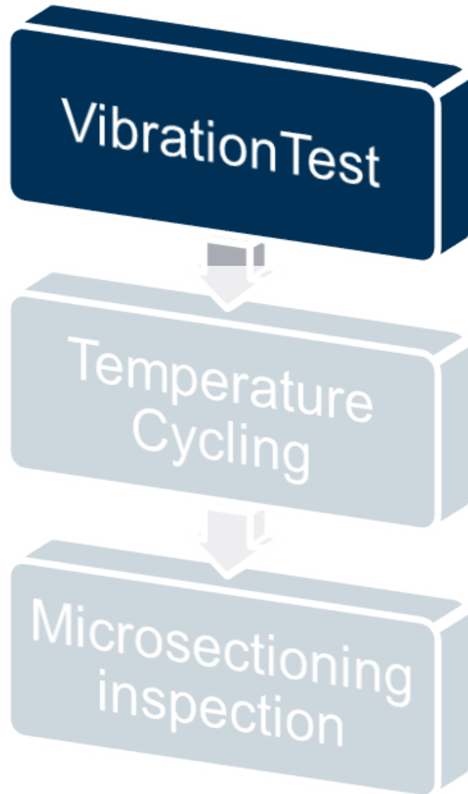


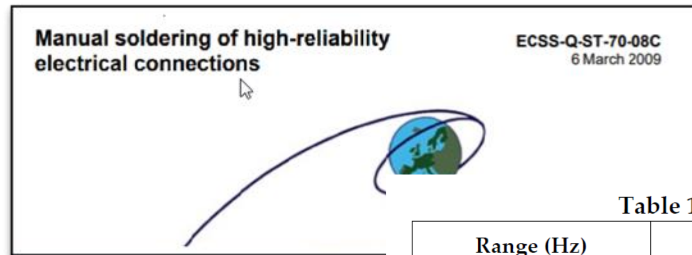




EXPERIMENTAL PROCEDURE

Test Flow

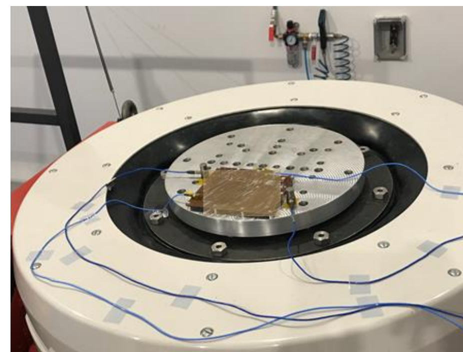


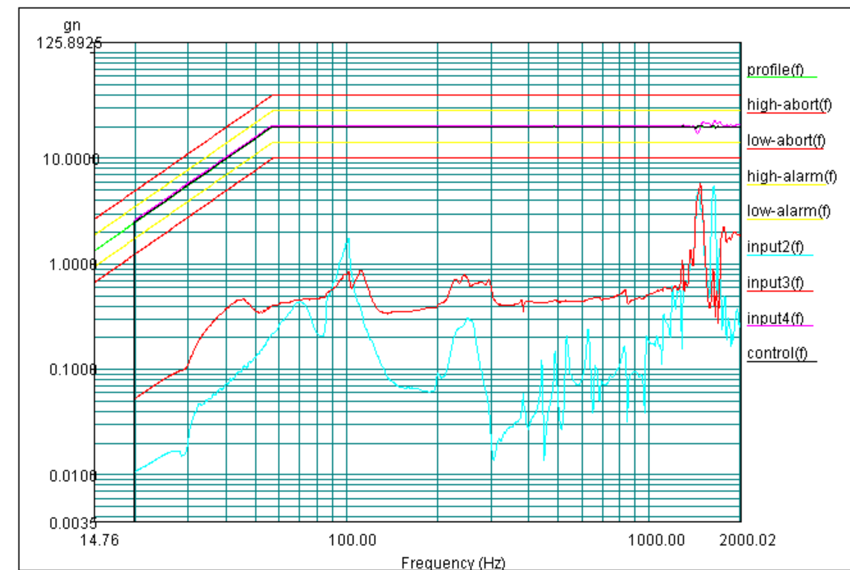

Manual soldering of high-reliability electrical connections

ECSS-Q-ST-70-08C
6 March 2009

Table 13-2: Minimum severity for sine vibration testing

Range (Hz)	PSD Level (0 to peak)	Sweep rate (Oct/ min)
Spacecraft		
25 to 100	20g	1
100 to 200	15g	
Duration: 1 cycle up from 25Hz to 200Hz		





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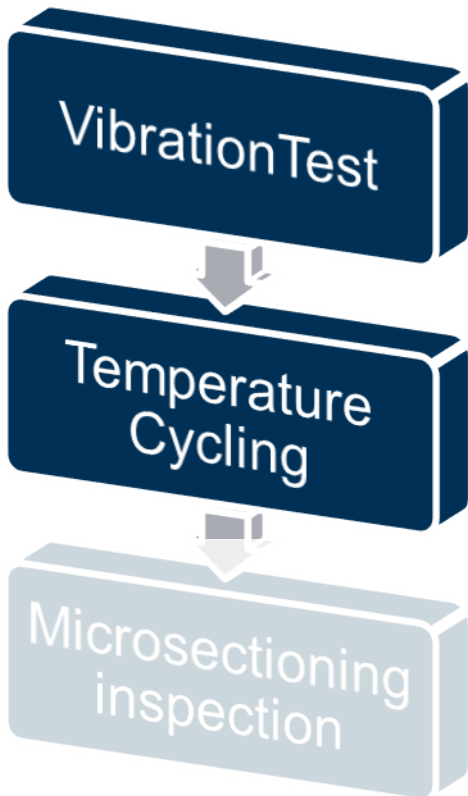
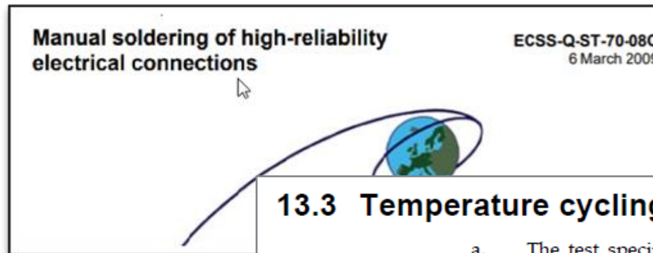
Test Flow




Manual soldering of high-reliability electrical connections

ECSS-Q-ST-70-08C
6 March 2009

13.3 Temperature cycling

a. The test specimen shall be temperature cycled in an air circulating or inert gas purged oven.

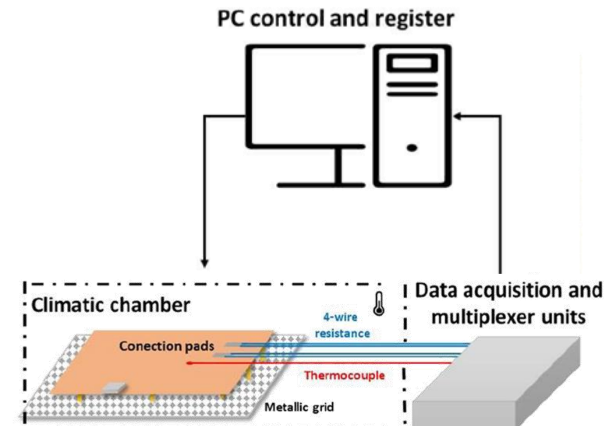
b. Before the start of the temperature cycling, the test specimen shall be baked-out to remove the internal humidity.

c. The bakeout temperature shall be between 60 °C and 80 °C"

d. The temperature cycle shall be between −55 °C and +100 °C

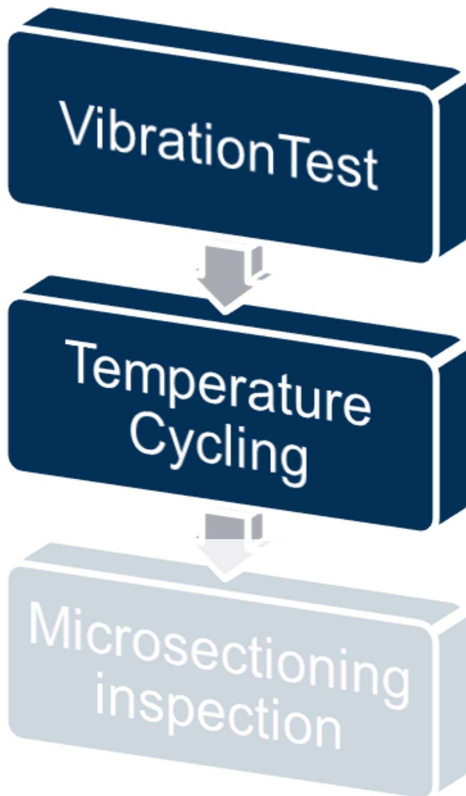
Temperature cycling test is defined by the following parameters:

- Baked-out temperature
- Number of cycles
- Max/Min temperature
- Dwell time
- **Temperature ramp**



EXPERIMENTAL PROCEDURE

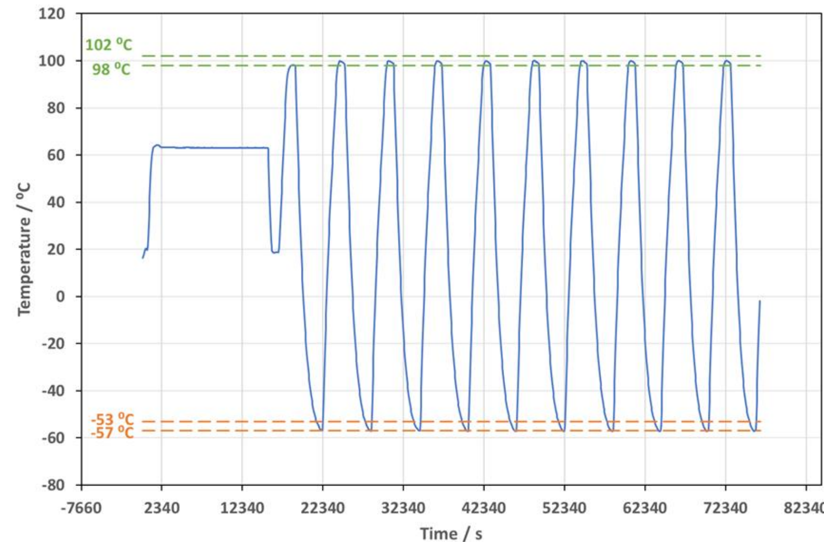
Test Flow



Ramp Temperature Condition:

Ramp 1 > Ramp 2

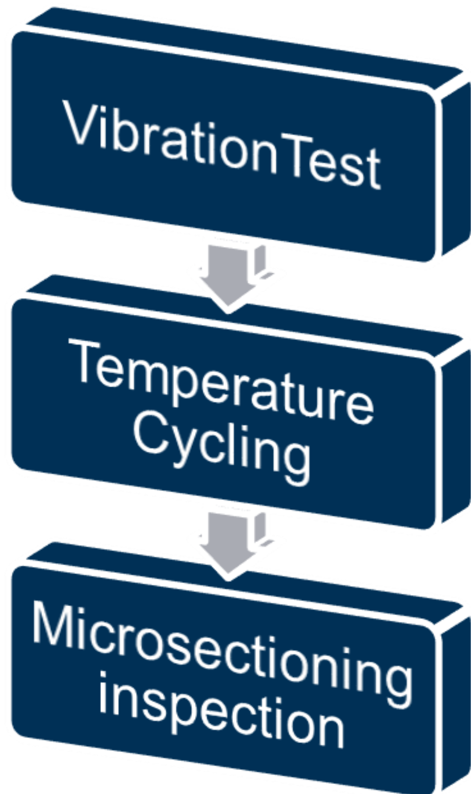
The temperature profile was monitoring in order to record any deviation:

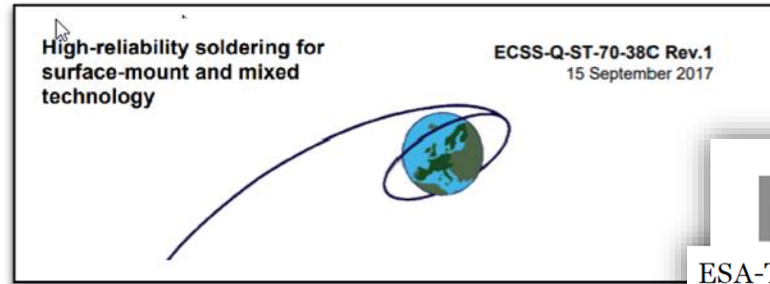


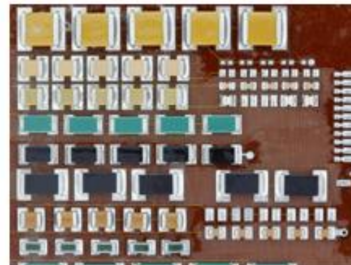
Control software

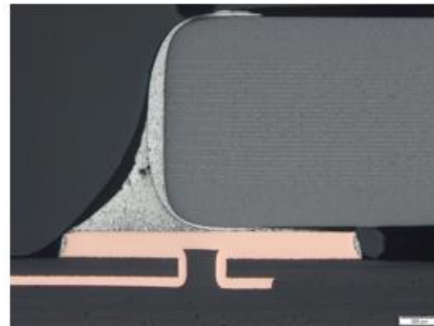
EXPERIMENTAL PROCEDURE

Test Flow

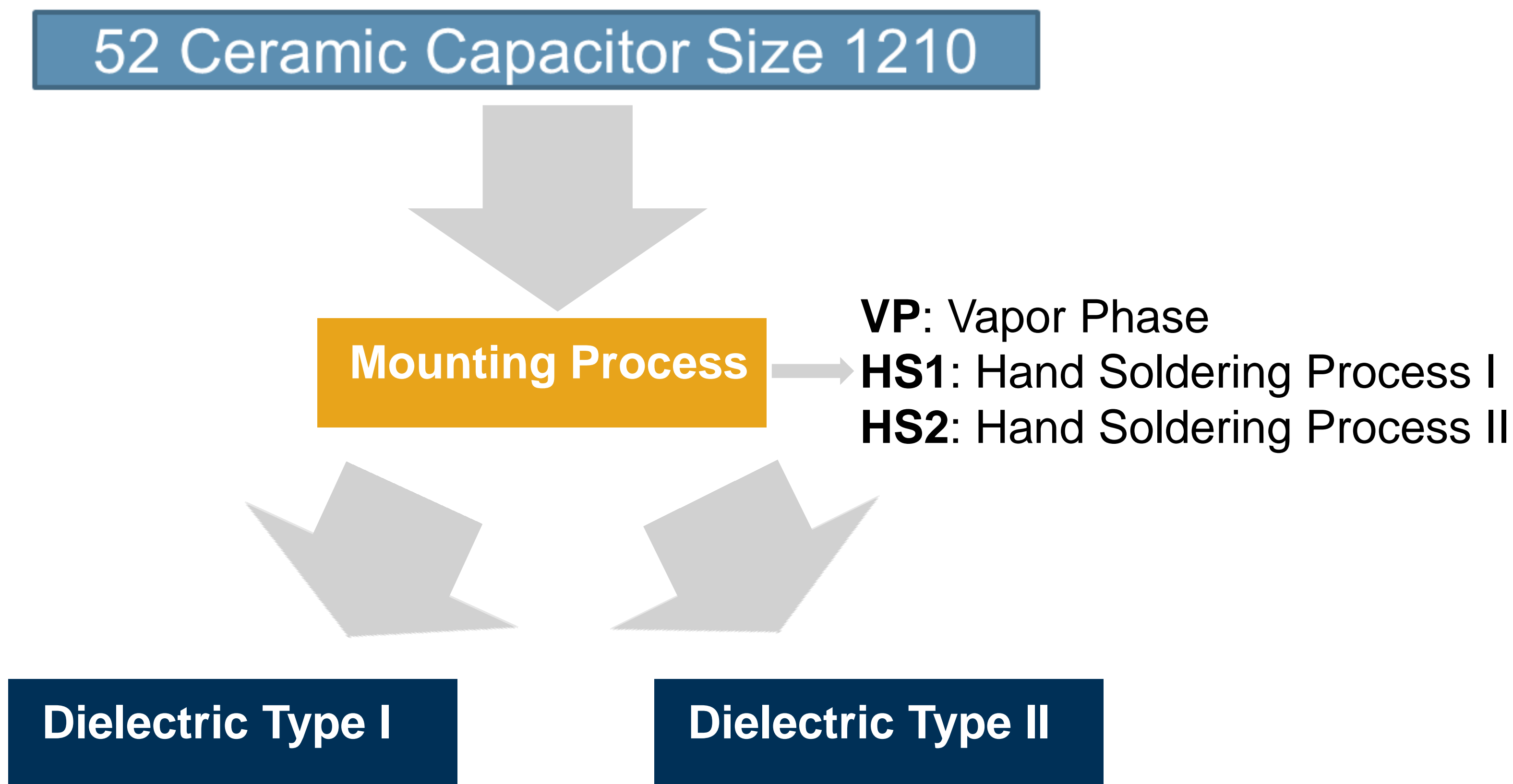








EXPERIMENTAL RESULTS



EXPERIMENTAL RESULTS

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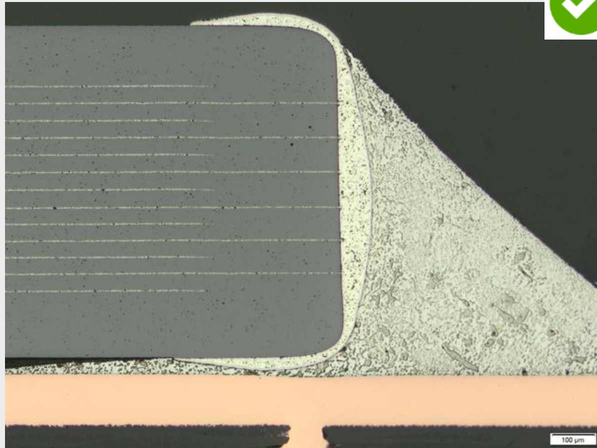
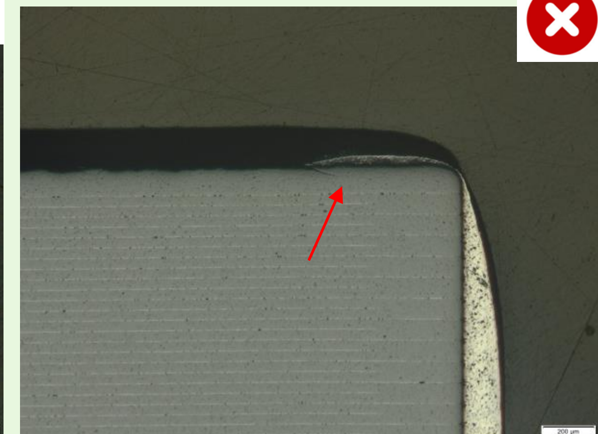
VP Process

Type I



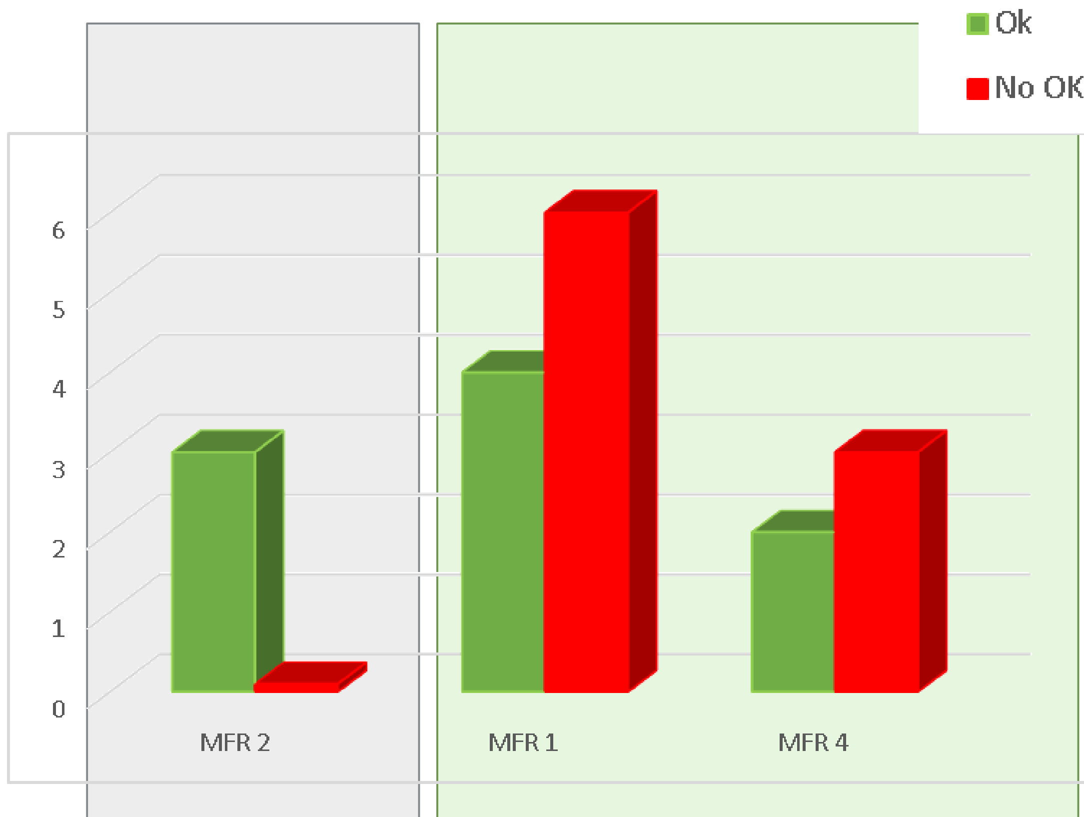
Type II



- **Type I**: No cracks.
- **Type II**: Some capacitors present cracks in the upper corner.

EXPERIMENTAL RESULTS

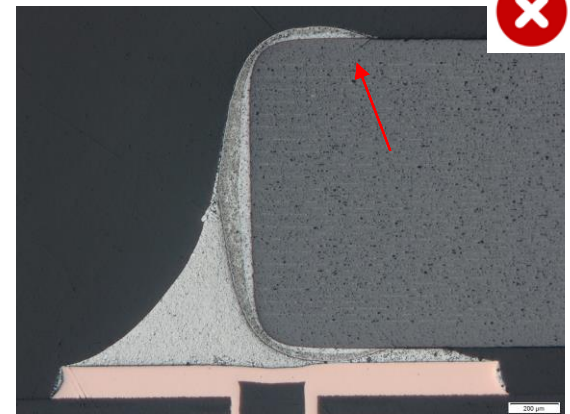
VP Process



Previous test results:
Type I: MFR 1, 3 & 4 ok
Type II: MFR 2 & 3 ok

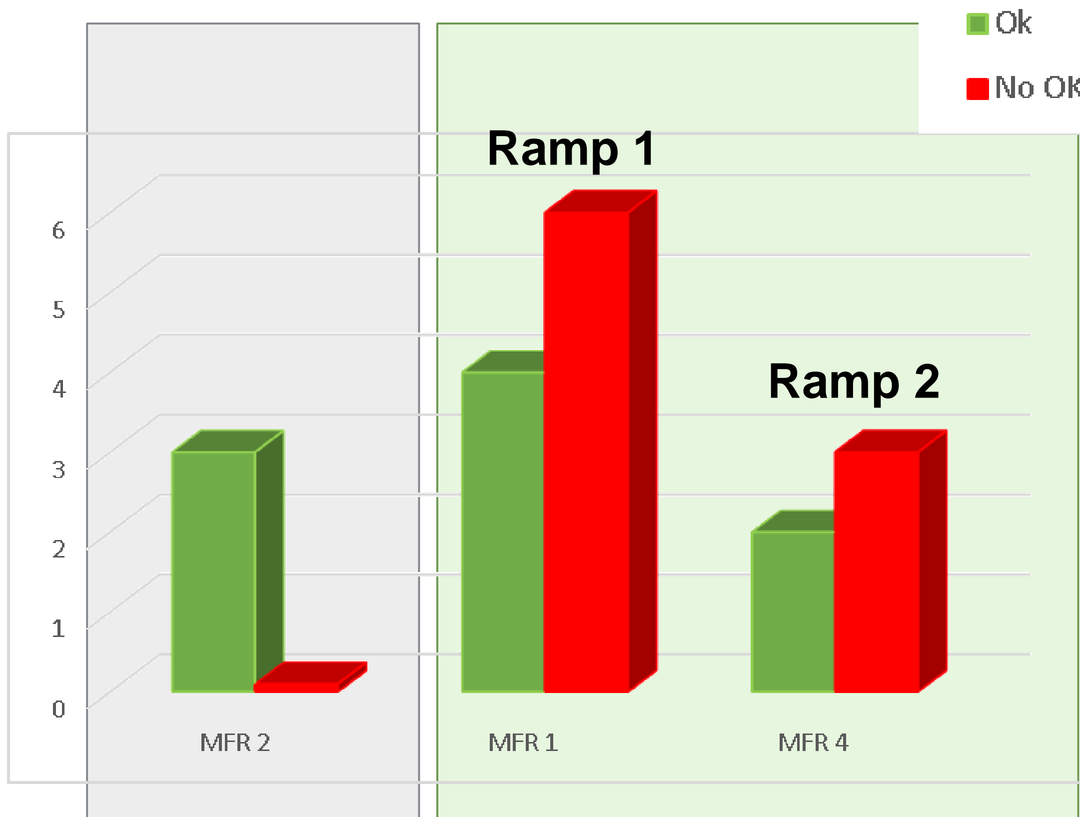
Type I: **OK**
Type II: **Results are linked to manufacturer.**

- **MFR 1**: 6 out of 10 capacitors with micro cracks on the top of the component
- **MFR 4** (with polymer protection layer): 3 out of 5 with micro crack on the top



EXPERIMENTAL RESULTS

VP Process



Previous test results:
Type I: MFR 1, 3 & 4 ok
Type II: MFR 2 & 3 ok

Type I: **OK**
Type II: **Results are linked to manufacturer.**

- **MFR 1**: 6 out of 10 capacitors with micro cracks on the top of the component
- **MFR 4** (with polymer protection layer): 3 out of 5 with micro crack on the top
- **No significant differences** between **ramp 1** and **ramp 2**.

EXPERIMENTAL RESULTS

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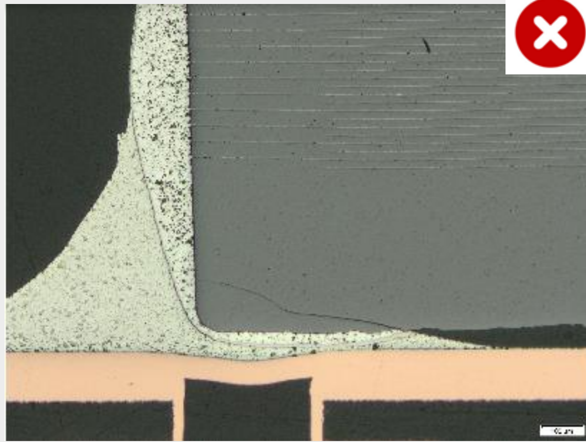
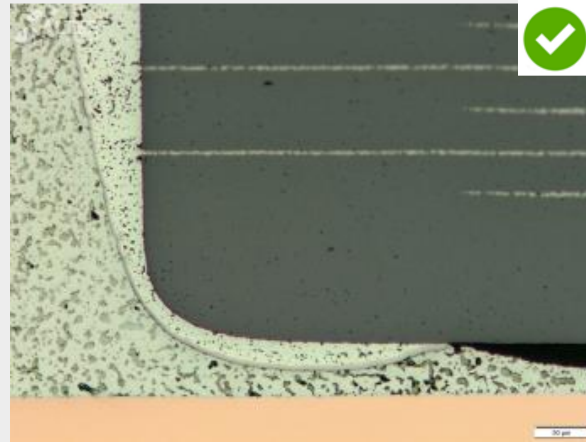
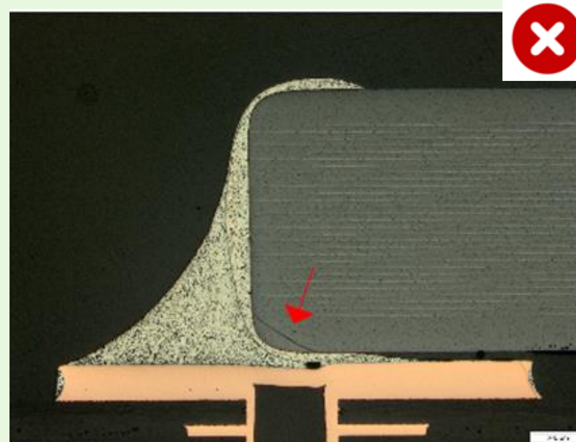
HS Process I

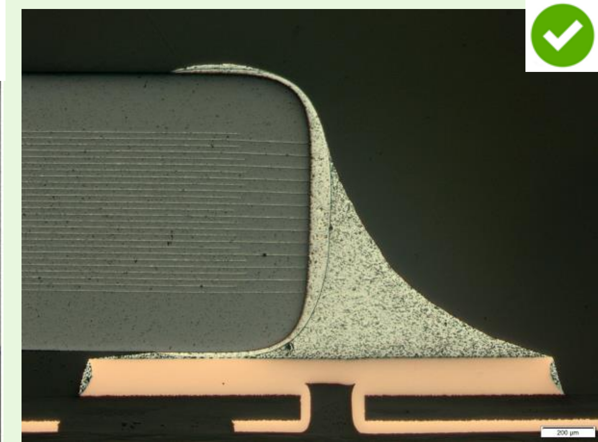
Type I





Type II



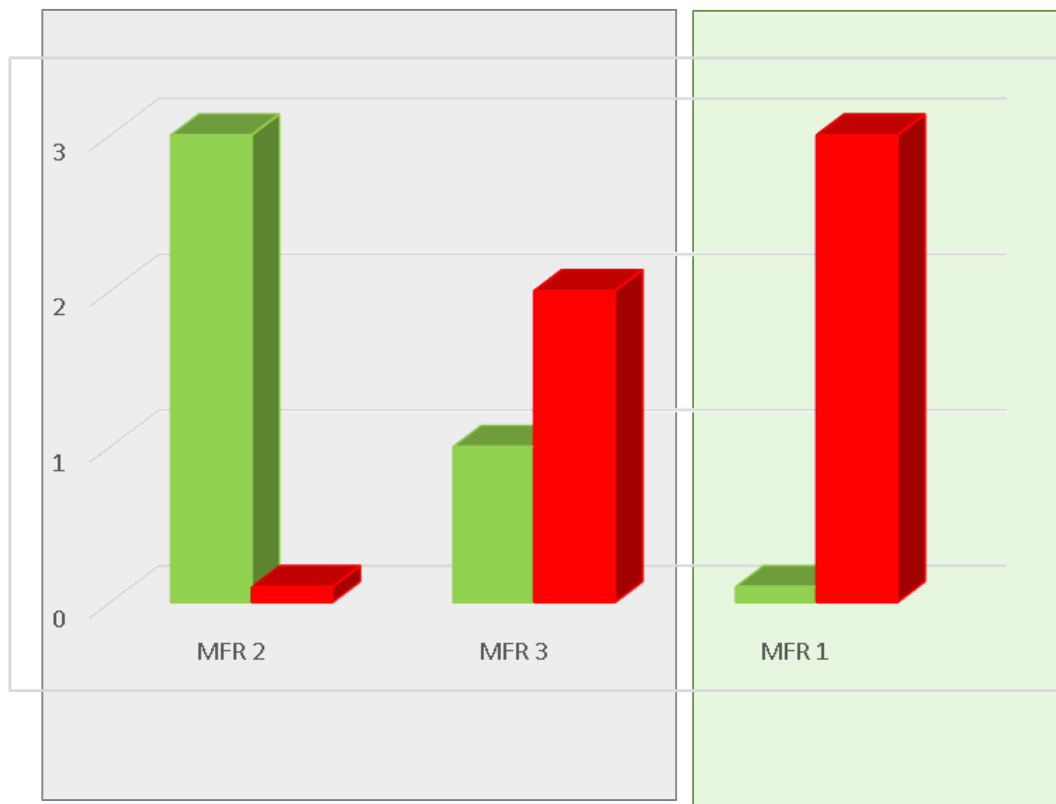


- **Type I**: Some capacitors present cracks.
- **Type II**: Some capacitors present cracks.

EXPERIMENTAL RESULTS

HS Process I Type I

Ramp 1 | Ramp 2

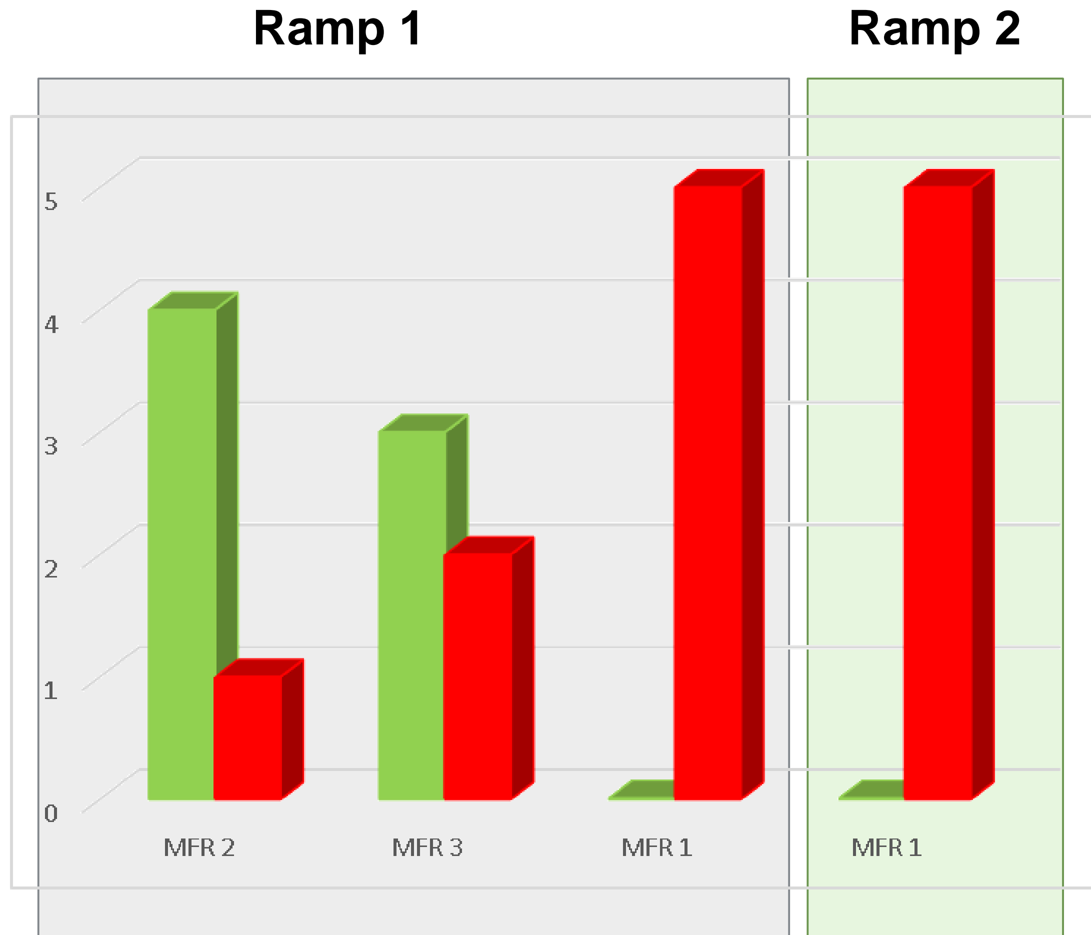


Type I: results are linked to manufacturer.

- **MFR 2**: OK.
- **MFR 3**: 2 out of 3 capacitors with crack in the ceramic.
- **MFR 1**: 3 out of 3 with crack in the ceramic.
- **No significant differences** between **ramp 1** and **ramp 2**.

EXPERIMENTAL RESULTS

HS Process I Type II



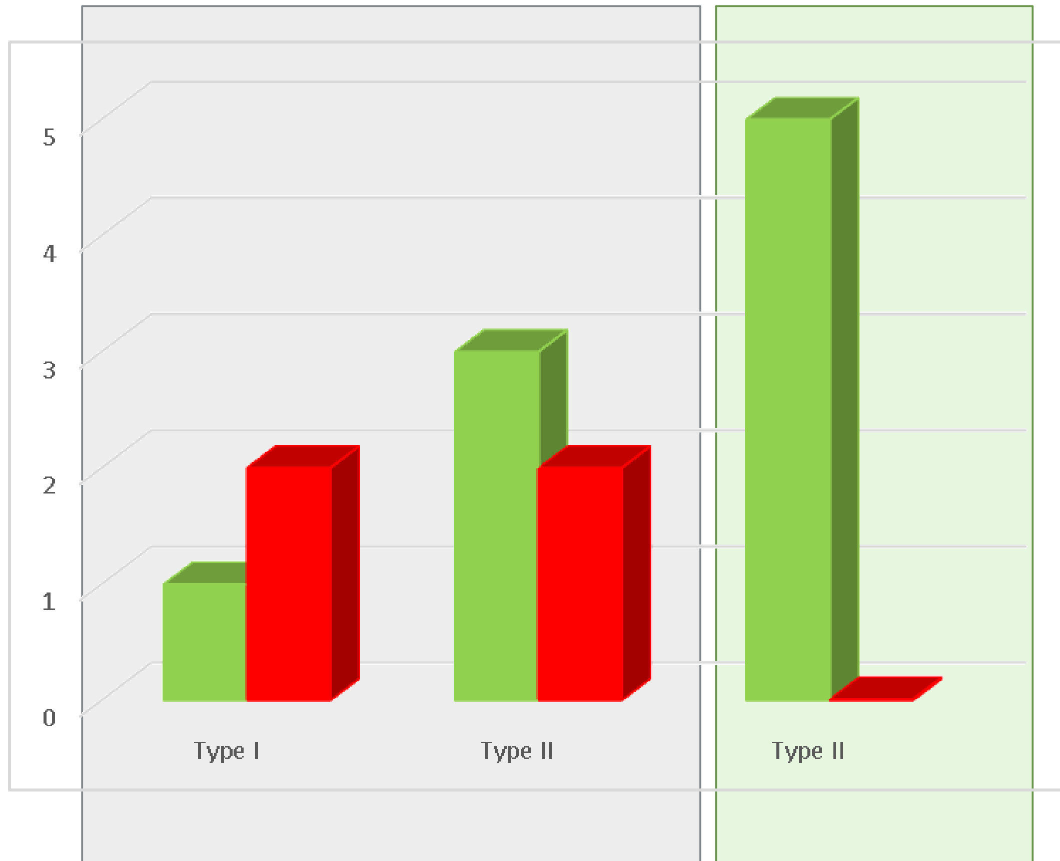
Type II: results are linked to manufacturer.

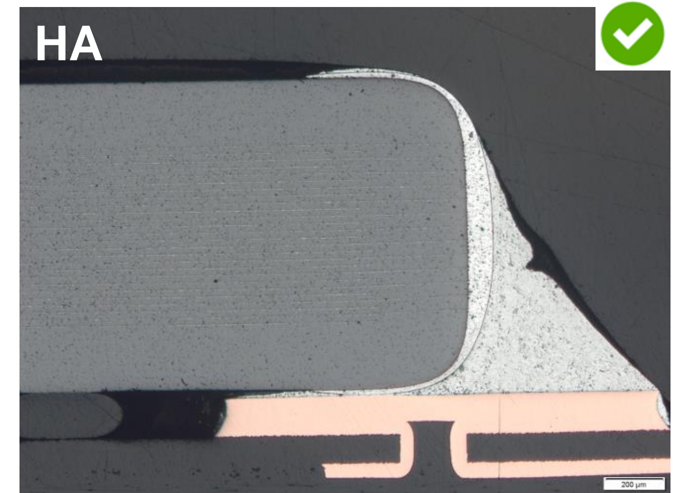
No satisfactory results

- **MFR 2**: 1 out of 5 with crack in the ceramic.
- **MFR 3**: 2 out of 5 with crack in the ceramic.
- **MFR 1**: 5 out 5 failed.
- **No differences** between **ramp 1** and **ramp 2**.

EXPERIMENTAL RESULTS

HS Process II MFR 3





Hand Soldering process II: satisfactory results

Comparison between type I and type II HS1 and HS2 for the same manufacturer **MFR3**

CONCLUSIONS

VP configuration:

Type I OK

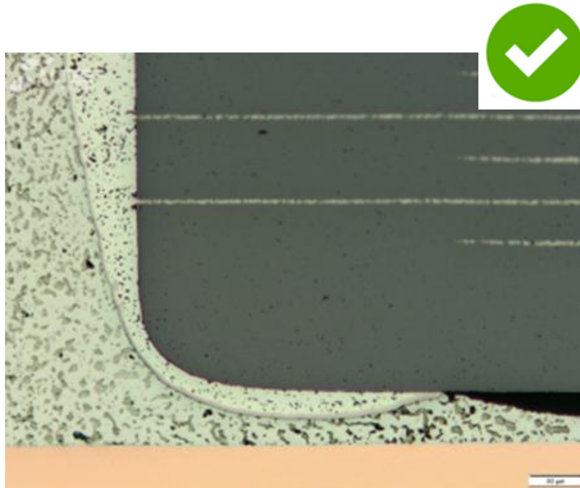
Type II Results are linked to manufacturer. Micro cracks on the top in some manufacturers. Others OK.

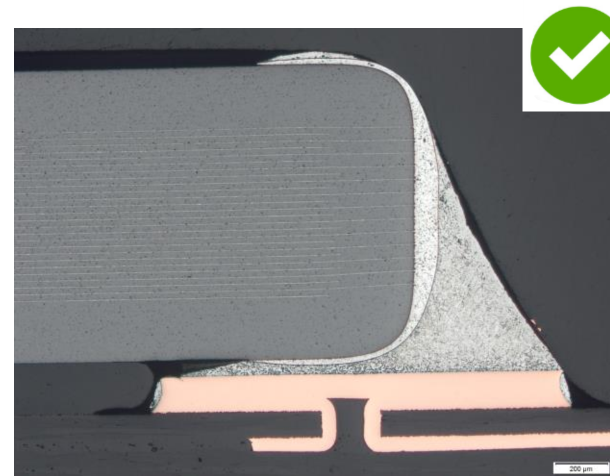
HS1 configuration:

Type I and **Type II** Results are linked to manufacturer. Cracks in ceramic bigger than in VP.

HS2 configuration:

The results for Hand soldering process II have been satisfactory.





THANK YOU!

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