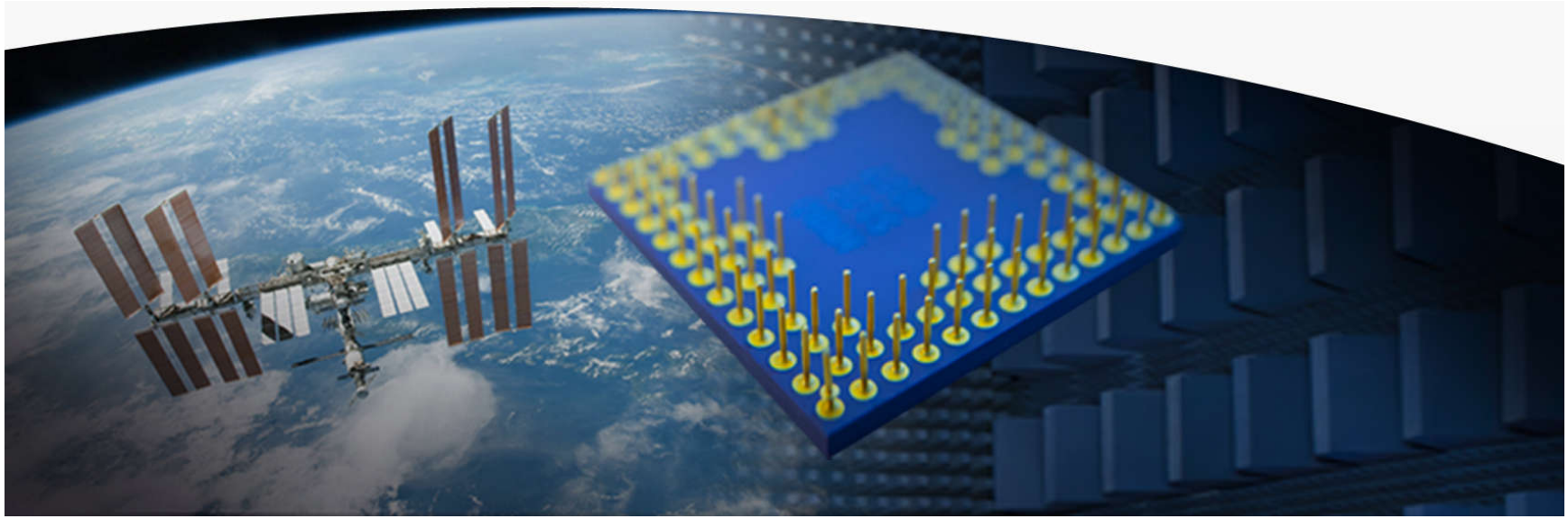


ASIC DESIGN SUPPORT CAPABILITIES

Sevilla, 14.03.2019

Sonia Vargas-Sierra, Head of Mixed Signal Test Development

sonia.vargas@altertechnology.com

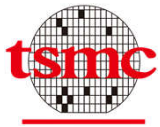
ALTER TECHNOLOGY

ASIC DESIGN SUPPORT OFFERED

- Staff for external workforce or support of ASIC development teams (**no ownership of licenses, connection via VPN or similar to design server**).
- Designers of over 10 years of experience in ASIC design: Analog, Mixed Signal and Digital Flows, RF simulation.
- Digital Design and Signoff: Full custom digital layouts, Front-End and Back-End flow and scripts, RTL development in Verilog or VHDL, functional simulation, constraint development, design for test logic, synthesis, timing analysis, power analysis, behavioral modeling, and verification.
- Custom IC/Analog: DRC, LVS, Custom Layouts, Ocean scripts, Skill Programming, Spectre, Spectre RF and Spectre AMS simulations, Verilog-A and Verilog-AMS behavioral models, corner and sweeps analysis, Monte Carlo statistical analysis, pre and post layout analysis.
- Optoelectronic design such as CMOS Image Sensors design including pixel design, on-chip processing and column-parallel ADCs.
- Pre-design mathematical models of the design via Matlab.
- Design For Test (DFx) consulting, particularly for very complex ASIC intended to be tested in High-End Automatic Test Equipments (ATE).

PREVIOUS EXPERIENCE IN ENVIRONMENTS AND TECHNOLOGIES

- Environments:
  - Cadence Design Environment:
    - Analog: Virtuoso Analog Design Environment Suite, Virtuoso Layout Suite, etc.
    - Digital: Encounter, etc.
    - Mixed: both analog and digital, including Spectre AMS
    - RF Simulations: Spectre RF
- Technologies:
  - AMS 0.35 µm normal and opto
  - UMC 0.18 µm normal and CIS
  - TSMC 65nm Low Power
  - Towerjazz 0.18 µm CIS.
  - Tezzaron FaStackTM (Chartered 130nm Low Power tiers 3D Integration)



ASIC DESIGNERS SUMMARIZED EXPERIENCE

- **Sonia Vargas-Sierra** received the Ph.D. degree in Microelectronics from the University of Seville in 2012. She has 10 years of experience in design and test of ASICs, particularly Smart High Dynamic Range (HDR) CMOS Image Sensors, Vision Systems-On-Chip (SOCs), and 3D Integrated Circuits for the Microelectronics Institute of Seville (IMSE-CNM). Currently, she is responsible of the Mixed Signal Test Development area of Alter Technology in Seville. During the last 4 years, she has accumulated experience in the development of test setups for the characterization of complex devices such as ASICs, Foundry Test ICs, Memories and High-Speed/High-Resolution ADCs/DACs to be qualified for space applications mainly for ESA projects. Expertise in High-End Automatic Test Systems (ATE) such as Teradyne UltraFlex, Applicos ATX7006 and Unites SZ M3000, which applies for Advanced Design For Test (DFT) ASIC design strategies.

- **Luis Carranza González** holds a PhD in Physics from the University of Seville. Since 1999, he has worked at IMSE-CNM-CSIC in the design, development and testing of ASICs and Artificial Autonomous Vision Systems. Since 2012 he has worked at the same center in the design, development and testing of radiation-hardened ASICs and integrated critical systems for aerospace applications. During 2018 he has combined his work at CSIC with the position of leading digital designer in the company Space Submicron Electronic. He has worked in research and/or development projects with ESA, NASA, CERN, INTA, Volvo Car Corporation, Fagor Automation, Anafocus, Derpom, ST-Microelectronics, University of Santiago de Compostela, Polytechnic University of Madrid, Polytechnic University of Cartagena, the University of Leuven and the LHCb-RICH group of the Department of Physics and Earth Sciences of the University of Ferrara.

- **M. Ángeles Jalón** received her B. Sc. Degree in Physics speciality in Electronic in 2001 from the University of Seville, Spain. In 2005 she received the Master of Advanced Studies in Microelectronics from the University of Seville, Spain. From 2003 to 2012 she was part of the Mixed-Signal group of the Institute of Microelectronics of Seville (IMSE) from the Spanish National Research Council (CSIC), operating variety of semiconductor processing and testing in development fabrication of prototype, custom-designed, electronic circuitry chips in research laboratory, and using knowledge of microelectronic processing equipment, procedures and also specifications. During this period, she published conference and journal works in the area of ADC characterization. She is currently working as Test Developer in the Mixed-Signal area and finishing her Ph. Degree (ADC test) in Alter Technology in Seville.

DESIGNERS RELEVANT PUBLICATIONS (1)

- "**CMOS Rad-Hard Front-End Electronics for Precise Sensors Measurements**", S. Sordo-Ibáñez, B. Piñero-García, M. Muñoz-Díaz, A. Ragel-Morales, J. Ceballos-Cáceres, L. Carranza-González, S. Espejo-Meana, A. Arias-Drake, J. Ramos-Martos, J.M. Mora-Gutierrez and M.A. Lagos-Florido, IEEE Transactions on Nuclear Science, vol. 63, no. 4, pp. 2379-2389, 2016 , IEEE DOI: 10.1109/TNS.2016.2586140 ISSN: 0018-9499
- "**A Front-End ASIC for a 3-D Magnetometer for Space Applications by Using Anisotropic Magnetoresistors**", S. Sordo-Ibáñez, B. Piñero-García, M. Muñoz-Díaz,A. Ragel-Morales, J. Ceballos-Cáceres, L. Carranza-González, S. Espejo-Meana, A. Arias-Drake, J. Ramos-Martos, J.M. Mora-Gutiérrez and M.A. Lagos-Florido, IEEE Transactions on Magnetics, vo. 51, no. 1, article 4001804, 2015, DOI: 10.1109/TMAG.2014.2356976 ISSN: 0018-9464
- "**Four-channel self-compensating single-slope ADC for space environments**", S. Sordo-Ibáñez, S. Espejo-Meana, B. Piñero-García, A. Ragel-Morales, J. Ceballos-Cáceres, M. Muñoz-Díaz, L. Carranza-González, A. Arias-Drake, J.M. Mora-Gutiérrez, M.A. Lagos-Florido and J. Ramos-Martos, Electronics Letters, vol. 50, no.8, pp 579-581, 2014, DOI: 10.1049/el.2014.0664 ISSN: 0013-5194.
- "**A Rad-Hard Multichannel Front-End Readout ASIC for Space Applications**", S. Sordo-Ibáñez, B. Piñero-García, M. Muñoz-Díaz, A. Ragel-Morales, J. Ceballos-Cáceres, L. Carranza-González, S. Espejo-Meana, A. Arias-Drake, J. Ramos-Martos, J.M. Mora-Gutiérrez and M.A. Lagos-Florido, IEEE International Workshop on Metrology for Aerospace METROAEROSPACE 2014.
- "**An Adaptive Approach to On-Chip CMOS Ramp Generation for High Resolution Single-Slope ADCs**", S. Sordo-Ibanez, B. Piñero-García, S. Espejo-Meana, A. Ragel-Morales, J. Ceballos-Cáceres, M. Muñoz-Díaz, L. Carranza-González, A. Arias-Drake, J.M. Mora-Gutiérrez and M.A. Lagos-Florido, European Conference on Circuit Theory and Design ECCTD 2013.
- "**Design Methodology and Development of Mixed-Signal ASICs for Space Applications in Standard CMOS Technology**", S. Sordo-Ibáñez, B. Piñero-García, M. Muñoz-Díaz, A. Ragel-Morales, J. Ceballos-Cáceres, L. Carranza-González, S. Espejo-Meana, A. Arias-Drake, J. Ramos-Martos, J.M. Mora-Gutiérrez and M.A. Lagos-Florido, IEEE/IFIP International Conference on VLSI and System-on-Chip VLSI-SoC 2013.
- "**A Front-End ASIC for a 16-Bit Three-Axis Magnetometer for Space Applications Based on Anisotropic Magnetoresistors**", S. Sordo-Ibáñez, B. Piñero-García, M. Muñoz-Díaz, A. Ragel-Morales, J. Ceballos-Cáceres, L. Carranza-González, S. Espejo-Meana, A. Arias-Drake, J. Ramos-Martos, J.M. Mora-Gutiérrez and M.A. Lagos-Florido, Conference on the Design of Circuits and Integrated Systems DCIS 2013.
- G. Liñán-Cembrano, L. Carranza-González, S. Espejo-Meana, R. Domínguez-Castro and A. Rodríguez-Vázquez, Book Chapter - **Smart Adaptive Systems on Silicon**, pp 103-118, 2004, SPRINGER DOI: 10.1007/978-1-4020-2782-6_7 ISBN: 978-1-4757-1051-9.

DESIGNERS RELEVANT PUBLICATIONS (2)

- "**A 151 dB High Dynamic Range CMOS Image Sensor Chip Architecture With Tone Mapping Compression Embedded In-Pixel**", S. Vargas-Sierra, G. Linán-Cembrano, A. Rodríguez-Vázquez, Sensors Journal, IEEE , vol.15, no.1, pp.180,195, Jan. 2015.
- "**A tone mapping algorithm for acquisition of high dynamic range images using event-driven adaptive digital CMOS pixels**", S. Vargas-Sierra, G. Linan Cembrano, Rodriguez-Vazquez, December 2013, Volume 77, Issue 3, pp 401-413.
- "**A 148dB focal-plane tone-mapping QCIF imager**", S. Vargas-Sierra, G. Linan Cembrano, A. Rodriguez-Vazquez, A. Circuits and Systems (ISCAS) 2012, IEEE International Symposium on 2012, pp. 1616-1619.
- "**High-dynamic range tone-mapping algorithm for focal plane processors**", S. Vargas-Sierra, G. Linan-Cembrano, E. Roca, A. Rodriguez-Vazquez, Proc. SPIE 8068, Bioelectronics, Biomedical, and Bioinspired Systems V; and Nanotechnology V, 806807 (May 03, 2011).
- "**A 176×144 148dB adaptive tone-mapping imager**", S. Vargas-Sierra, G. Liñán-Cembrano, and A. Rodríguez-Vázquez, Proc. SPIE 8298, Sensors, Cameras, and Systems for Industrial and Scientific Applications XIII, 82980A (15 February 2012); doi: 10.1117/12.905240; https://doi.org/10.1117/12.905240.
- "**APS design alternatives in 0.18µm CMOS image sensor technology**", S. Vargas-Sierra, E. Roca and G. Liñán-Cembrano, 2009 European Conference on Circuit Theory and Design, Antalya, 2009, pp. 1-4, doi: 10.1109/ECCTD.2009.5275145.
- "**Form Factor Improvement of Smart-Pixels for Vision Sensors through 3-D Vertically-Integrated Technologies**", A. Rodríguez-Vázquez, R. Carmona-Galán, J. Fernández Berni, S. Vargas, J.A. Leñero, M. Suárez, V. Brea and B. Pérez-Verdú, IEEE Latin American Symposium on Circuits and Systems LASCAS 2014.
- "**Design of a smart camera SoC in a 3D-IC technology**", R. Carmona-Galán, J. Fernández-Berni, S. Vargas-Sierra, G. Liñán-Cembrano, A. Rodríguez-Vázquez, V. Brea-Sánchez, M. Suárez-Cambre and D. Cabello-Ferrer, Workshop on Architecture of Smart Camera, 2012.
- "**A 2.5GHz Bandpass Active Complex Filter with 2.4MHz Bandwith for Wireless Communications**", Jose Antonio Villegas, Diego Vázquez, Adoración Rueda, Antonio Ginés, Ricardo Roldán, Eduardo Peralías, Mª Ángeles Jalón, Antonio Acosta, Rafaella Bianca, Design of Circuits and Integrated Systems 2008 (DCIS 2008), Genoble, Francia. ISBN: 978-2-84813-124-5, pp 18-23.
- "**A 1.2V 5.14mW Quadrature Frequency Synthesizer in 90nm CMOS Technology for 2.4GHz ZigBee Applications**", A.J. Ginés, R. Roldan, A. Villegas, A.J. Acosta, M.A. Jalón, D. Vázquez, A. Rueda, E. Peralías, IEEE Asia Pacific Conference on Circuits and Systems 2008 (APCCAS 2008), Macao, China. ISBN: 978-1-4244-2342-2, pp 1252-1255.

THANK YOU!